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MS-7A72

Intel -Kabylake plamform Z270 / H270 / B250

ATX

Ver: 1.0

CPU:

Kabylake-S

System Chipset:

Z270 Colay H270 and B250

Onboard Chip:

HD Audio Codec : ALC887

LAN : Intel I219

SIO : Nuvoton 6795

Flash ROM : 16MB GSE Z270

8MB GSE Lite For H270 / B250

Main Memory:

DDRIV (800/1066/1333/1600/2133MHz) * 4 (Dual Channel)

ACPI:

NIKO/UPI

PWM:

RT3606BC

Expansion Slots:

PCI Express (X16) Slot *1

PCI Express (X4) Slot * 1

PCI Express (X1) Slot * 3

PCI Slot * 1

M2 * 2 (22110 and 2280)

Other:

SATA3.0 x6 (PCH)

FRONT USB2.0 *4

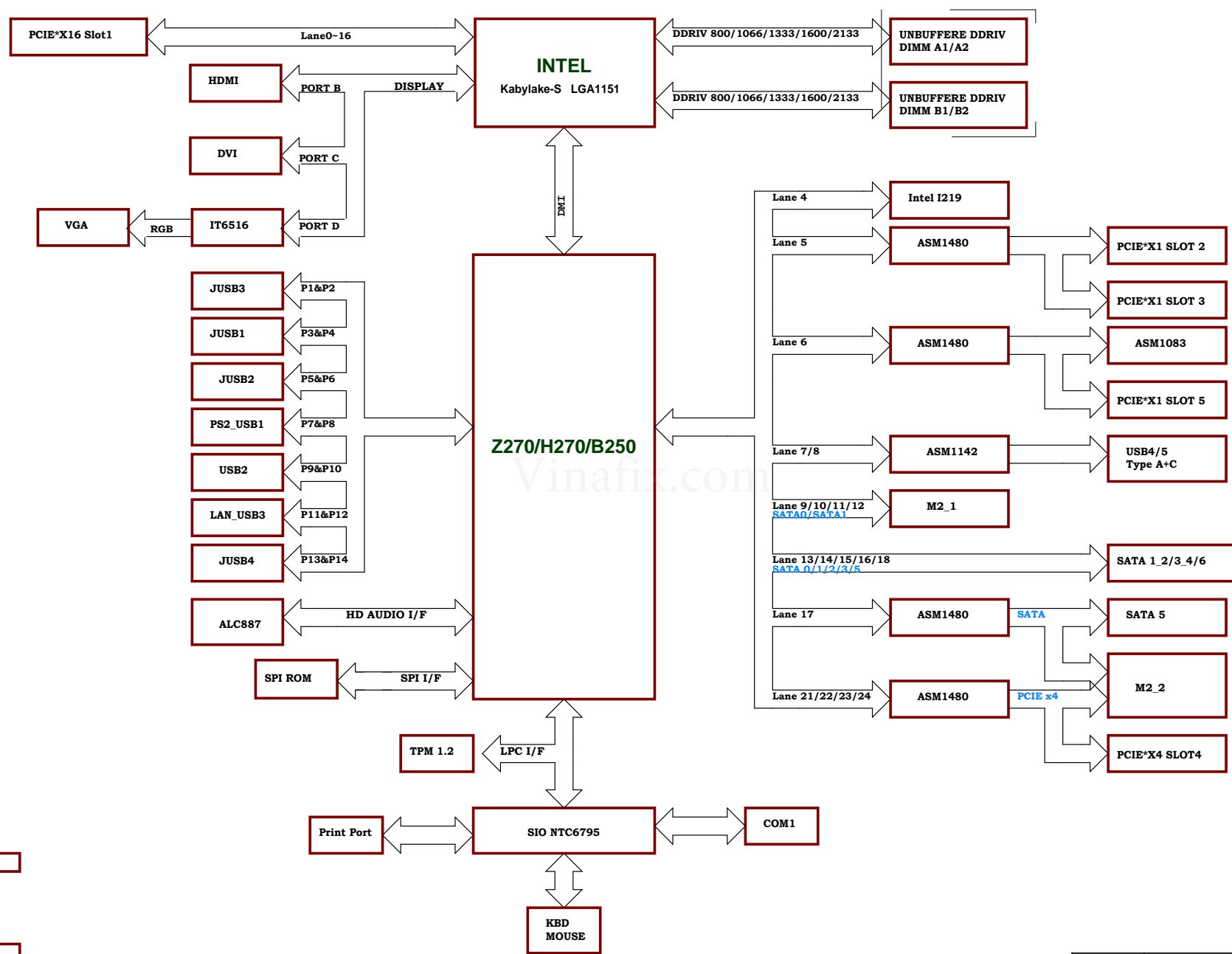
FRONT USB3.0 *4(B250 only 2)

REAR USB2.0 *2

REAR USB3.0 *4

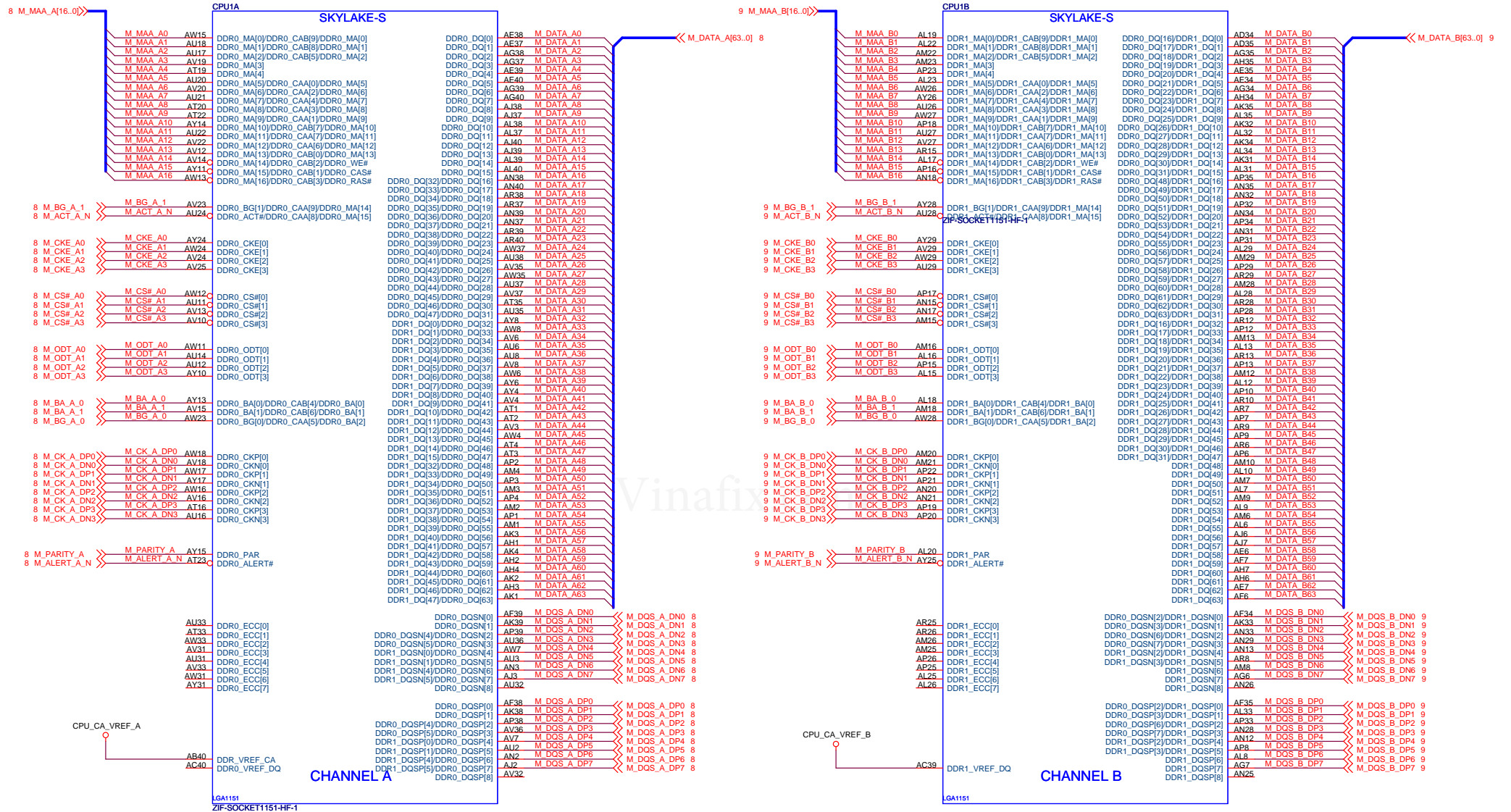
REAR USB3.1 TYPE A+C

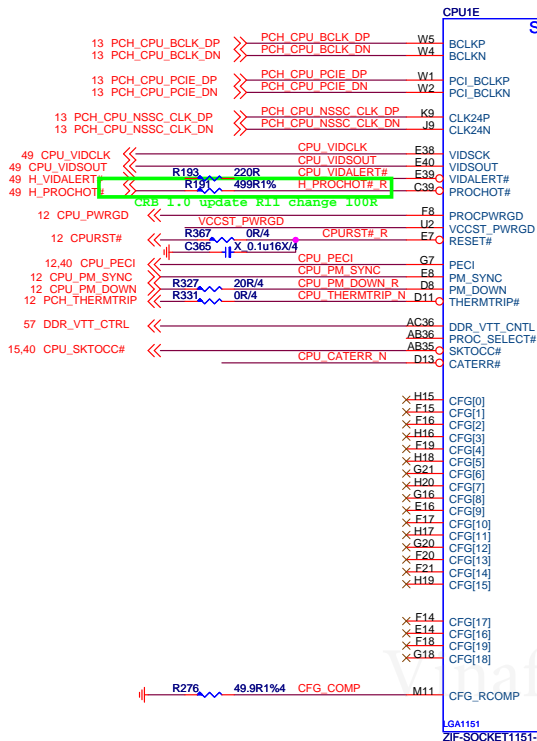
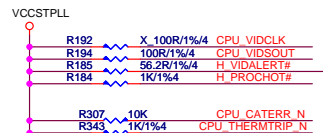
MS-7A72 Block Diagram



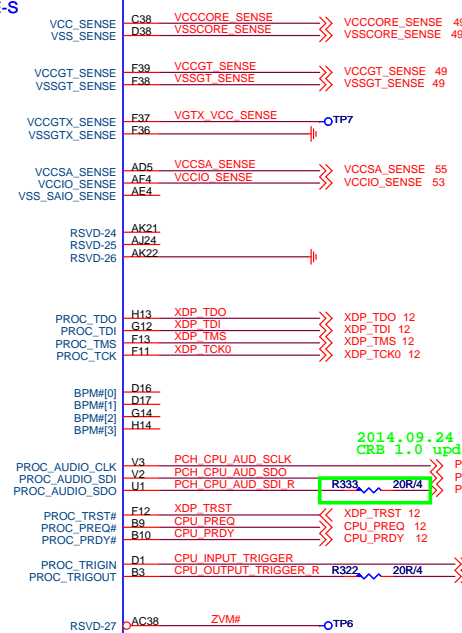
- Slot Sequence:
- PCIE X16
 - PCIE X1
 - PCIE X1
 - PCIE X4
 - PCIE X1
 - PCI

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SKYLAKE-S



CFG Strap

CFG Table

| | HIGH | LOW | DESCRIPTION |
|----|---------|----------|---------------------|
| 0 | No Lock | Lock | PCU PLL lock |
| 1 | RSVD | RSVD | RSVD |
| 2 | NORM | REVERSE | PEG LANE REVERSAL |
| 3 | RSVD | RSVD | RSVD |
| 4 | DISABLE | ENABLE | eDP |
| 5 | DISABLE | ENABLE | PEGCPSEL[0] |
| 6 | DISABLE | ENABLE | PEGCPSEL[1] |
| 7 | RESET# | BIOS REQ | PEG DEFERR TRAINING |
| 8 | RSVD | RSVD | RSVD |
| 9 | RSVD | RSVD | RSVD |
| 10 | RSVD | RSVD | RSVD |
| 11 | RSVD | RSVD | RSVD |
| 12 | RSVD | RSVD | RSVD |
| 13 | RSVD | RSVD | RSVD |
| 14 | RSVD | RSVD | RSVD |
| 15 | RSVD | RSVD | RSVD |

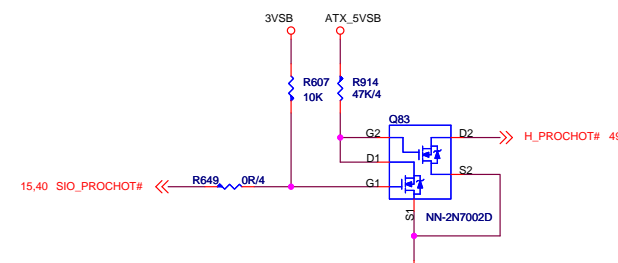
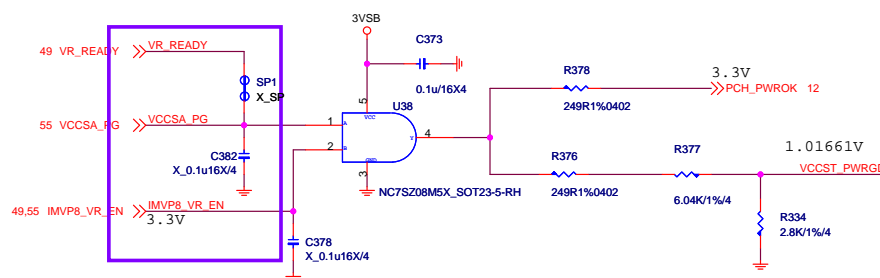
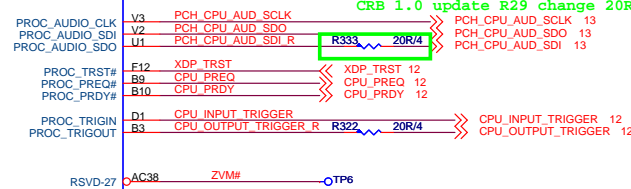
2014.09.29 remove

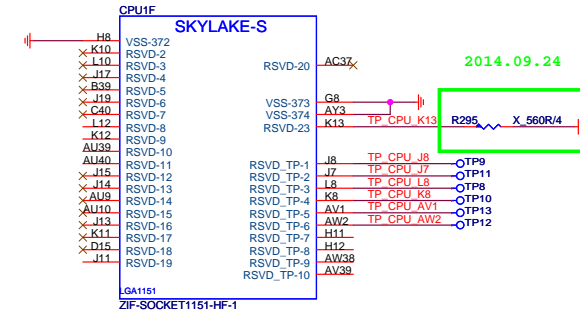
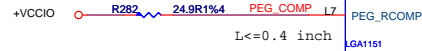
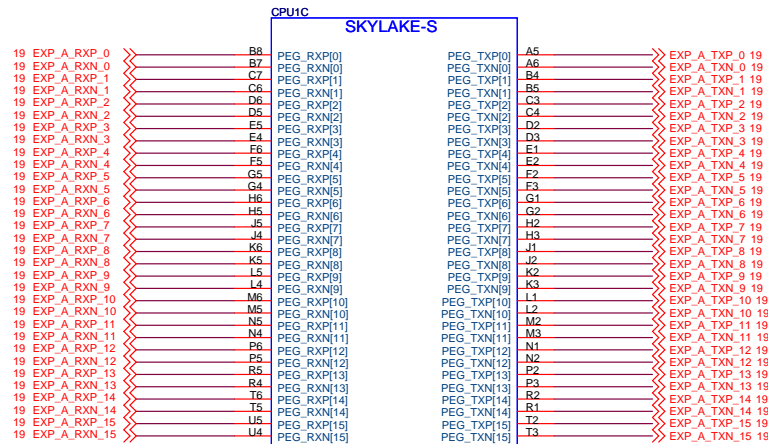


Close CPU <1100 mil

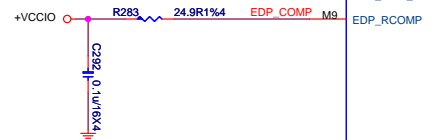
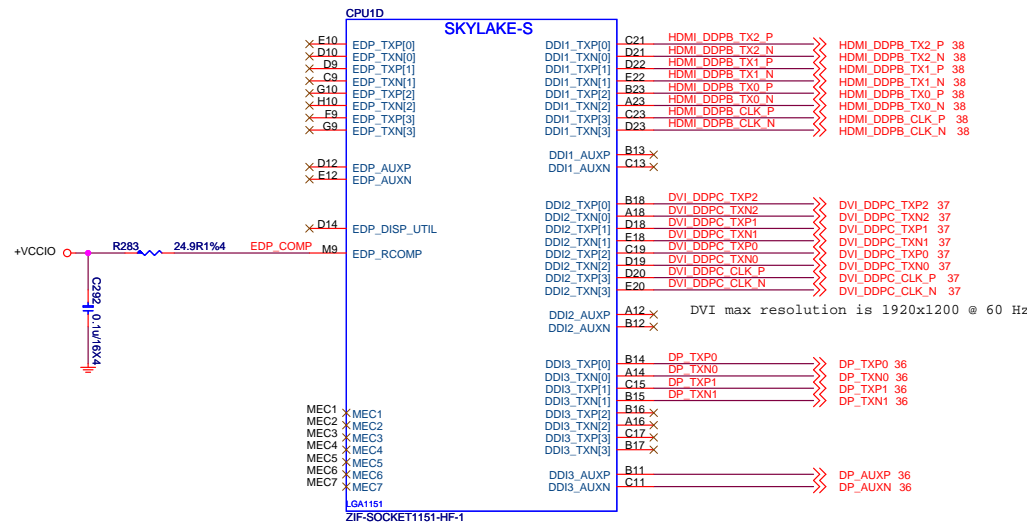
1000 mil < CPU_XDP_MBP0~1 < 6000 mil

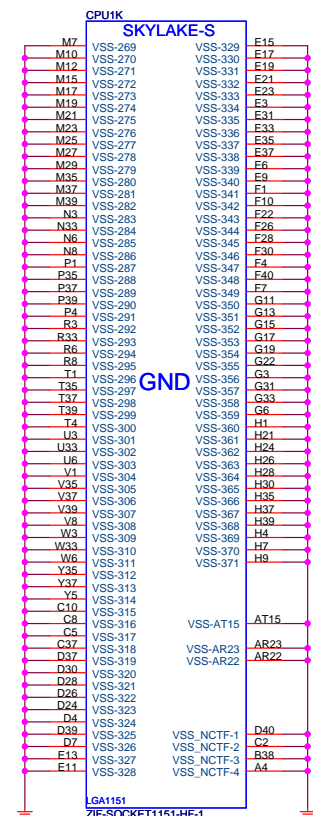
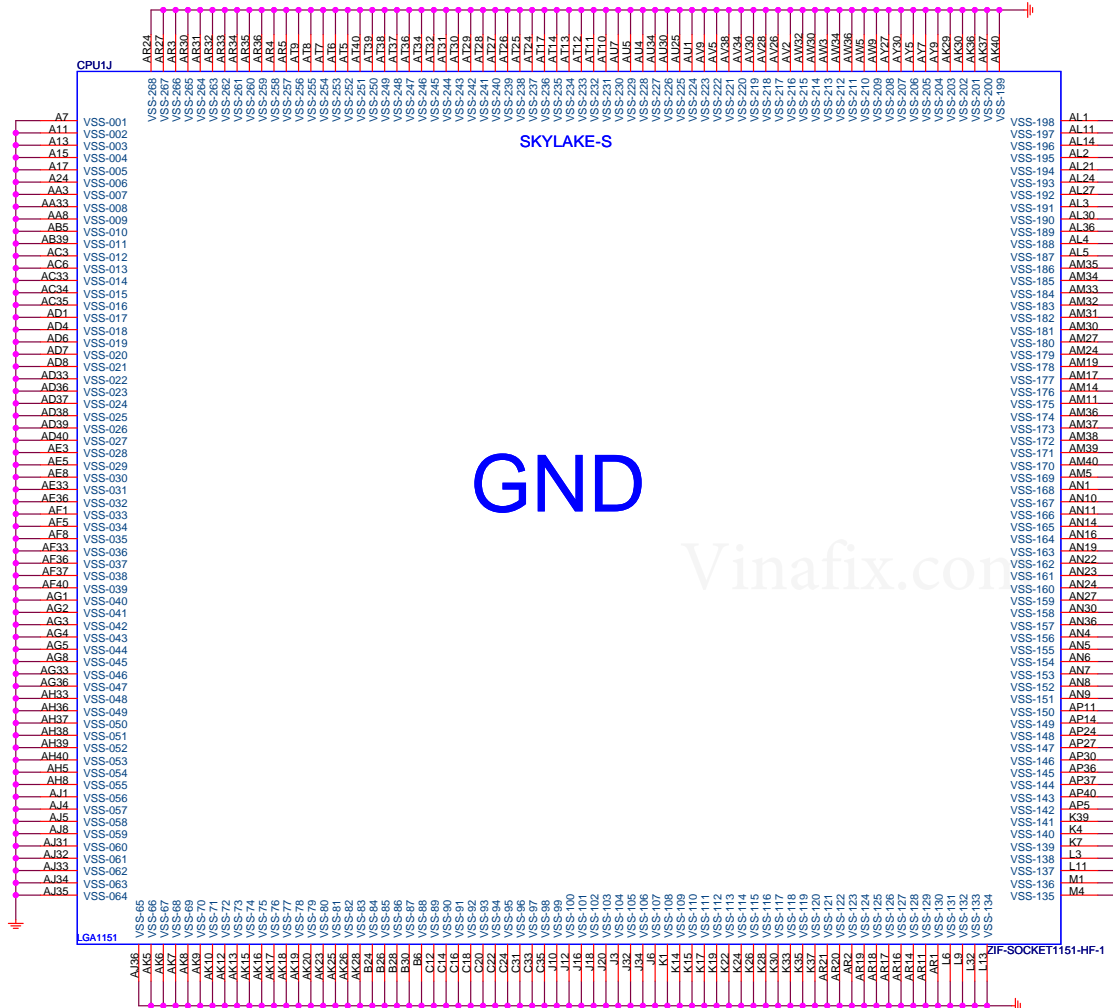
2014.09.24
CRB 1.0 update R29 change 20R

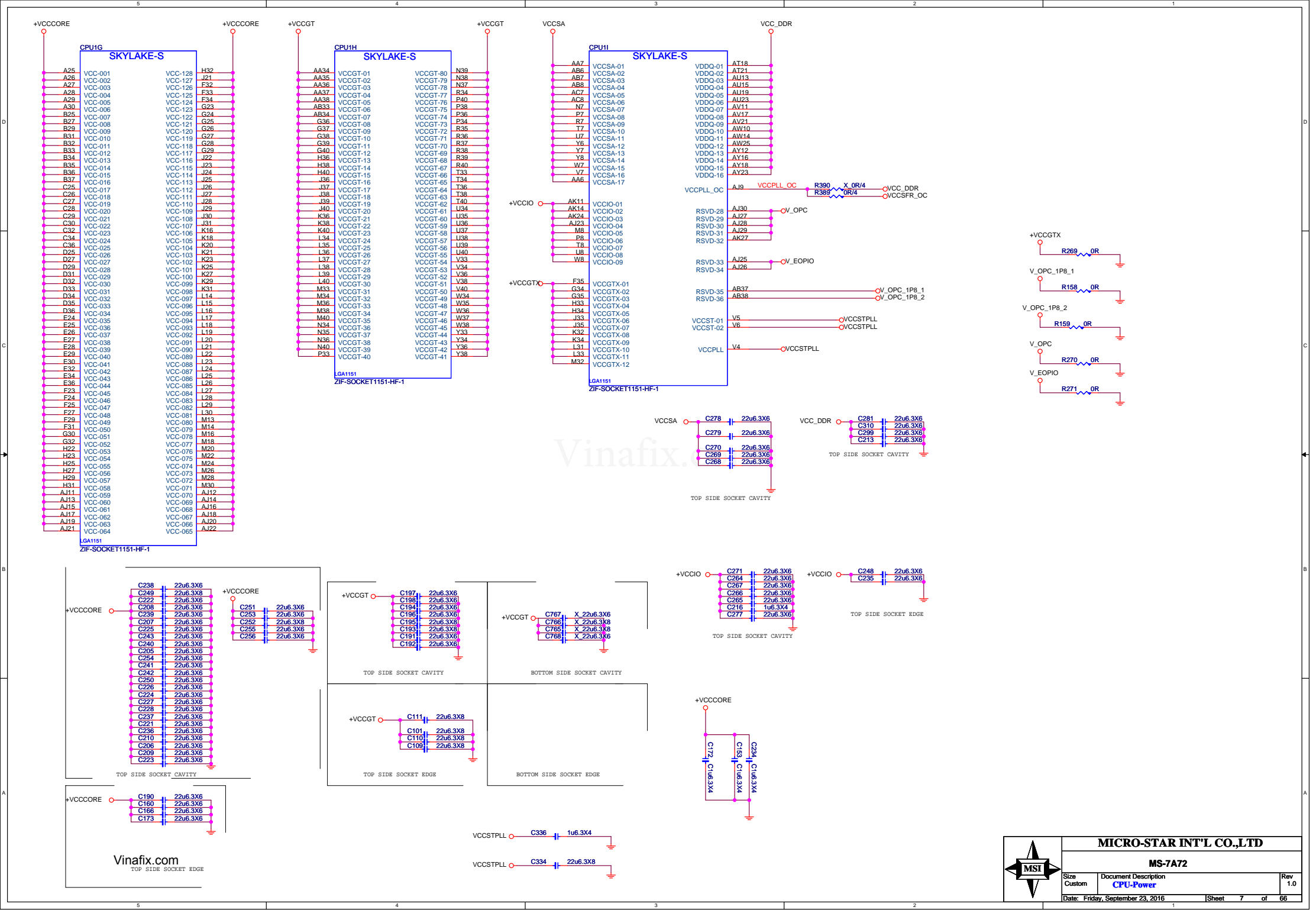


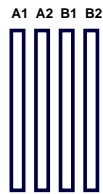


CRB 1.0 update
CRB unstuff
PCB come back remove









3 M_DQS_A_DP7 >> M_DQS_A_DP7 278
3 M_DQS_A_DN7 >> M_DQS_A_DN7 277
3 M_DQS_A_DP6 >> M_DQS_A_DP6 267
3 M_DQS_A_DN6 >> M_DQS_A_DN6 266
3 M_DQS_A_DP5 >> M_DQS_A_DP5 256
3 M_DQS_A_DN5 >> M_DQS_A_DN5 255
3 M_DQS_A_DP4 >> M_DQS_A_DP4 245
3 M_DQS_A_DN4 >> M_DQS_A_DN4 244
3 M_DQS_A_DP3 >> M_DQS_A_DP3 186
3 M_DQS_A_DN3 >> M_DQS_A_DN3 185
3 M_DQS_A_DP2 >> M_DQS_A_DP2 175
3 M_DQS_A_DN2 >> M_DQS_A_DN2 174
3 M_DQS_A_DP1 >> M_DQS_A_DP1 164
3 M_DQS_A_DN1 >> M_DQS_A_DN1 163
3 M_DQS_A_DP0 >> M_DQS_A_DP0 153
3 M_DQS_A_DN0 >> M_DQS_A_DN0 152
3 M_CK_A_DP1 >> M_CK_A_DP1 218
3 M_CK_A_DN1 >> M_CK_A_DN1 219
3 M_CK_A_DP0 >> M_CK_A_DP0 74
3 M_CK_A_DN0 >> M_CK_A_DN0 75
3 M_CS#_A1 >> S1_N 89
3 M_CS#_A0 >> S0_N 84
3 M_CKE_A1 >> CKE1 203
3 M_CKE_A0 >> CKE0 60
3 M_ODT_A1 >> ODT-1 91
3 M_ODT_A0 >> ODT-0 87
DIMM_RESET# 58
DIMM1_EVENT 78
3 M_ALERT_A_N >> M_ALERT_A_N 208
3 M_ACT_A_N >> M_ACT_A_N 62
3 M_PARITY_A >> M_PARITY_A 222
SAVE_N_NC 230
RFU-0 144
RFU-1 205
RFU-2 227

VCC_DDR
DQ-63 280 M_DATA_A57
DQ-62 135 M_DATA_A59
DQ-61 273 M_DATA_A61
DQ-60 128 M_DATA_A56
DQ-59 282 M_DATA_A60
DQ-58 137 M_DATA_A62
DQ-57 275 M_DATA_A58
DQ-56 130 M_DATA_A63
DQ-55 269 M_DATA_A55
DQ-54 124 M_DATA_A53
DQ-53 262 M_DATA_A48
DQ-52 117 M_DATA_A50
DQ-51 271 M_DATA_A49
DQ-50 126 M_DATA_A51
DQ-49 264 M_DATA_A52
DQ-48 119 M_DATA_A54
DQ-47 258 M_DATA_A42
DQ-46 113 M_DATA_A46
DQ-45 251 M_DATA_A40
DQ-44 106 M_DATA_A41
DQ-43 260 M_DATA_A43
DQ-42 115 M_DATA_A47
DQ-41 253 M_DATA_A44
DQ-40 108 M_DATA_A45
DQ-39 247 M_DATA_A39
DQ-38 102 M_DATA_A38
DQ-37 240 M_DATA_A37
DQ-36 95 M_DATA_A36
DQ-35 249 M_DATA_A35
DQ-34 104 M_DATA_A34
DQ-33 97 M_DATA_A33
DQ-32 188 M_DATA_A27
DQ-31 43 M_DATA_A30
DQ-30 181 M_DATA_A25
DQ-29 36 M_DATA_A28
DQ-28 190 M_DATA_A31
DQ-27 45 M_DATA_A26
DQ-26 183 M_DATA_A24
DQ-25 38 M_DATA_A29
DQ-24 177 M_DATA_A23
DQ-23 32 M_DATA_A19
DQ-22 170 M_DATA_A20
DQ-21 25 M_DATA_A21
DQ-20 179 M_DATA_A18
DQ-19 34 M_DATA_A22
DQ-18 172 M_DATA_A16
DQ-17 27 M_DATA_A17
DQ-16 166 M_DATA_A15
DQ-15 21 M_DATA_A11
DQ-14 159 M_DATA_A8
DQ-13 14 M_DATA_A9
DQ-12 168 M_DATA_A14
DQ-11 23 M_DATA_A10
DQ-10 161 M_DATA_A13
DQ-9 16 M_DATA_A12
DQ-8 155 M_DATA_A7
DQ-7 10 M_DATA_A3
DQ-6 148 M_DATA_A4
DQ-5 3 M_DATA_A1
DQ-4 157 M_DATA_A2
DQ-3 12 M_DATA_A6
DQ-2 150 M_DATA_A0
DQ-1 5 M_DATA_A5

C2 235
S3_N_C1 237
S2_N_C0 93
S1_N 89
S0_N 84
CKE1 203
CKE0 60
ODT-1 91
ODT-0 87
CB-7 199
CB-6 54
CB-5 192
CB-4 47
CB-3 201
CB-2 56
CB-1 194
CB-0 49
RESET_N 58
EVENT_N 78
ALERT_N 208
ACT_N 62
PAR 222
SAVE_N_NC 230
RFU-0 144
RFU-1 205
RFU-2 227

DDRIV-288P_BLACK-RH-21
DIMM1 (CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]

12 DRAM_RESET# >> R246 OR DIMM_RESET# >> DIMM_RESET# 9

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C167
X_0.1u16X/4

12 SMBCLK_VCC >> SMBCLK_VCC R387 OR SMB_CLK_DIMM >> SMB_CLK_DIMM 9
12 SMBDATA_VCC >> SMBDATA_VCC R388 OR SMB_DATA_DIMM >> SMB_DATA_DIMM 9

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DIMM1_EVENT R277 240R/4/1%
DIMM2_EVENT R278 240R/4/1%

3 M_CK_A_DP3 >> M_CK_A_DP3 218
3 M_CK_A_DN3 >> M_CK_A_DN3 219
3 M_CK_A_DP2 >> M_CK_A_DP2 74
3 M_CK_A_DN2 >> M_CK_A_DN2 75
3 M_CS#_A3 >> S1_N 89
3 M_CS#_A2 >> S0_N 84
3 M_CKE_A3 >> CKE1 203
3 M_CKE_A2 >> CKE0 60
3 M_ODT_A3 >> ODT-1 91
3 M_ODT_A2 >> ODT-0 87
DIMM_RESET# 58
DIMM2_EVENT 78
3 M_ALERT_A_N >> M_ALERT_A_N 208
3 M_ACT_A_N >> M_ACT_A_N 62
3 M_PARITY_A >> M_PARITY_A 222
SAVE_N_NC 230
RFU-0 144
RFU-1 205
RFU-2 227

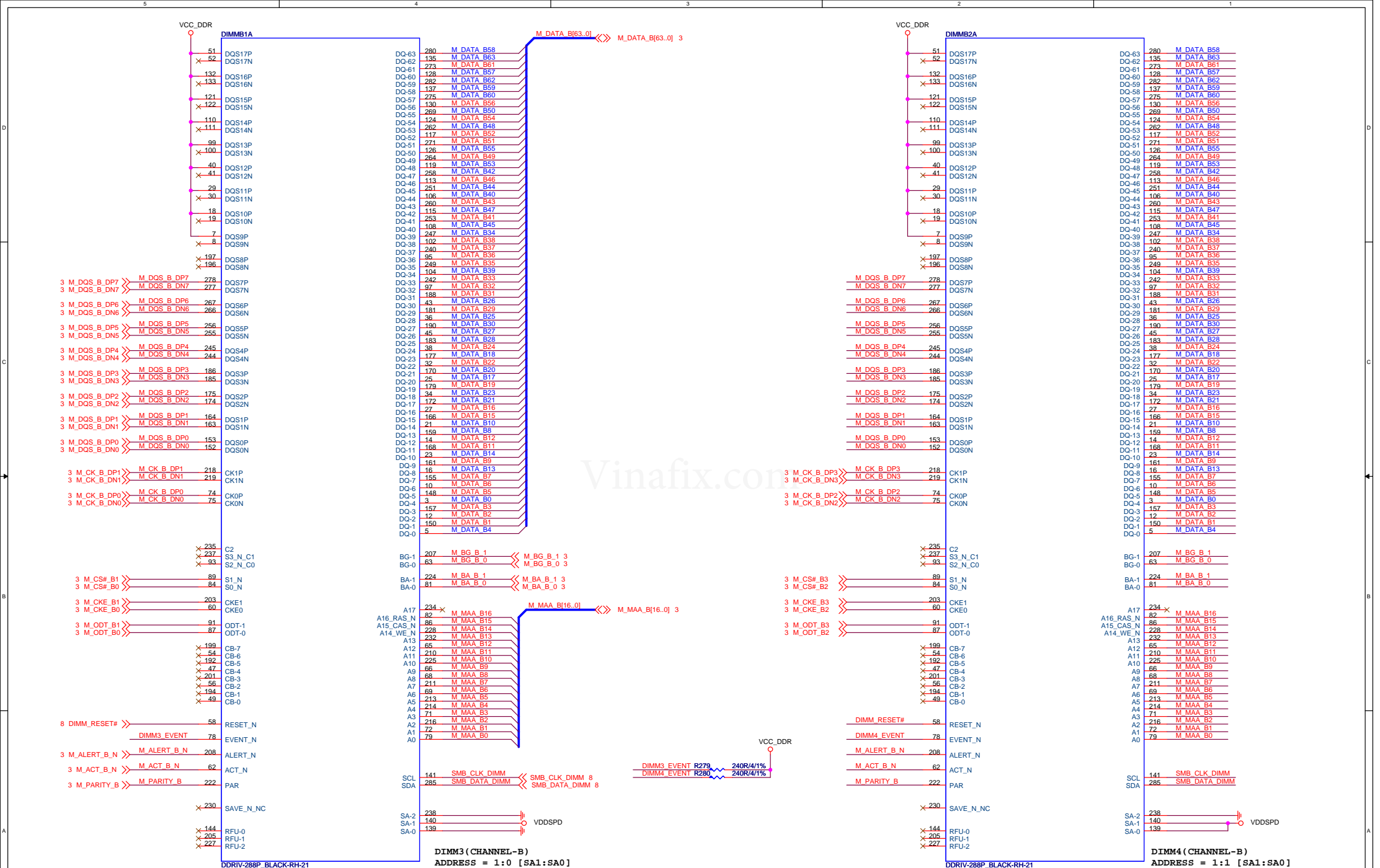
DDRIV-288P_BLACK-RH-21
DIMM2 (CHANNEL-A)
ADDRESS = 0:1 [SA1:SA0]

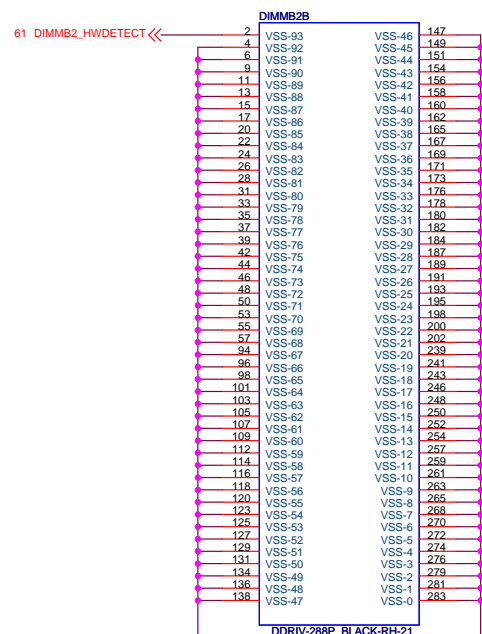
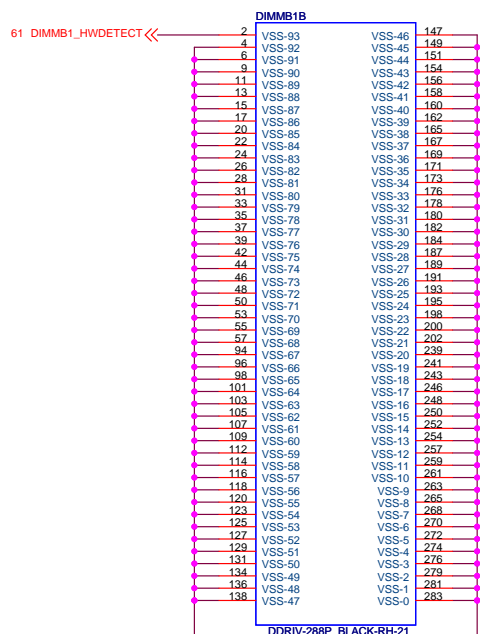
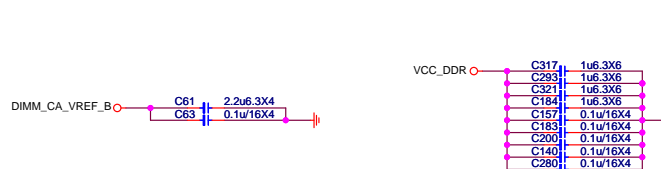
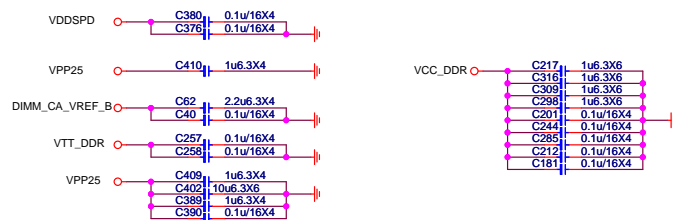
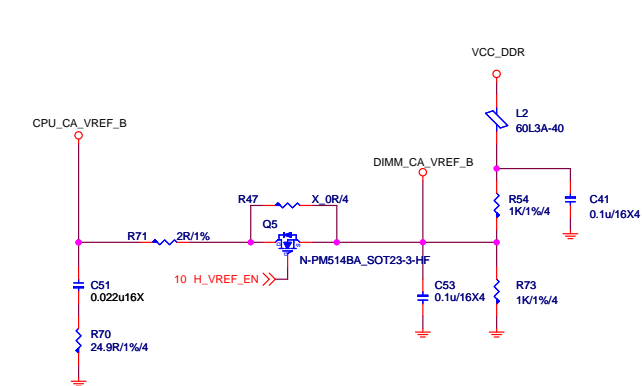
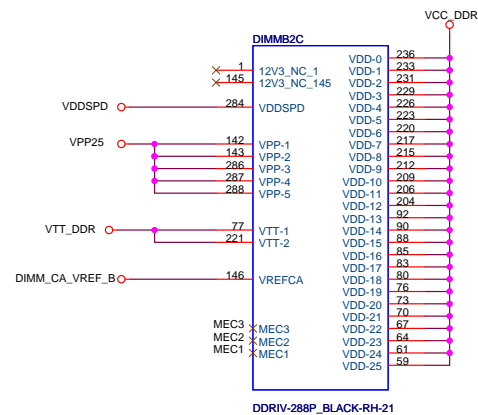
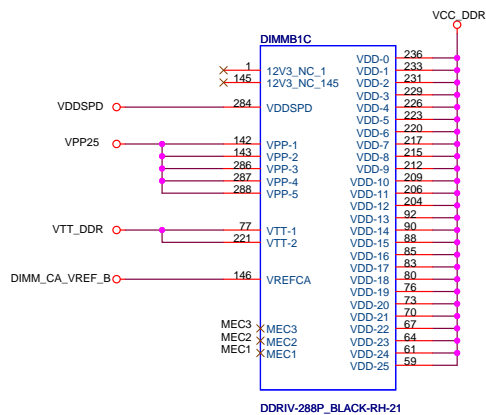


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MS-7A72

Size Custom Document Description DDR4 SLOT-DIMM1/DIMM2 Rev 1.0
Date: Friday, September 23, 2016 Sheet 8 of 66

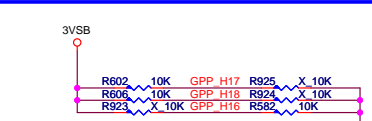
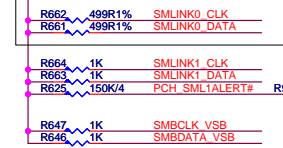




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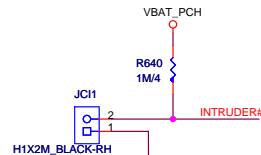


LANPHY USE by SPEC

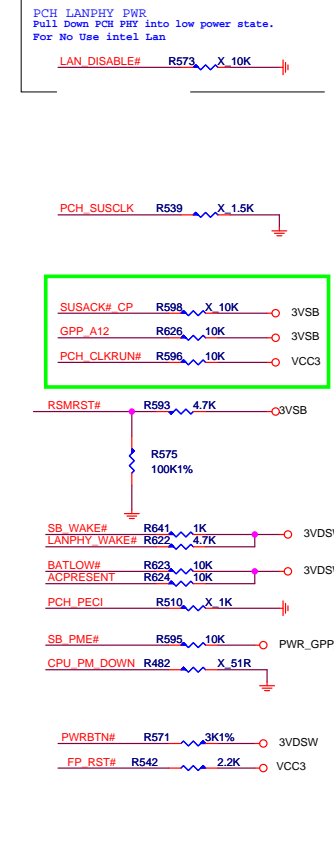
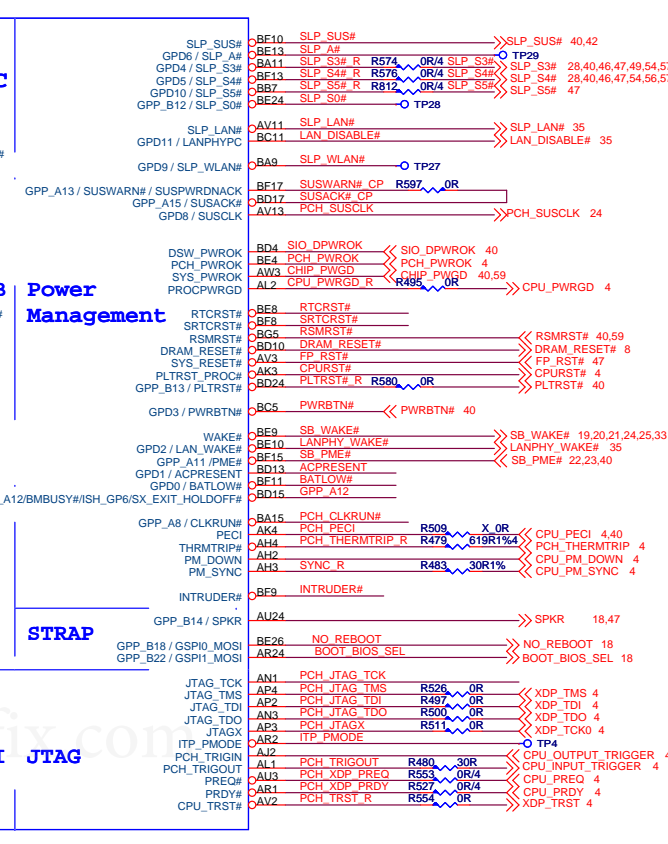
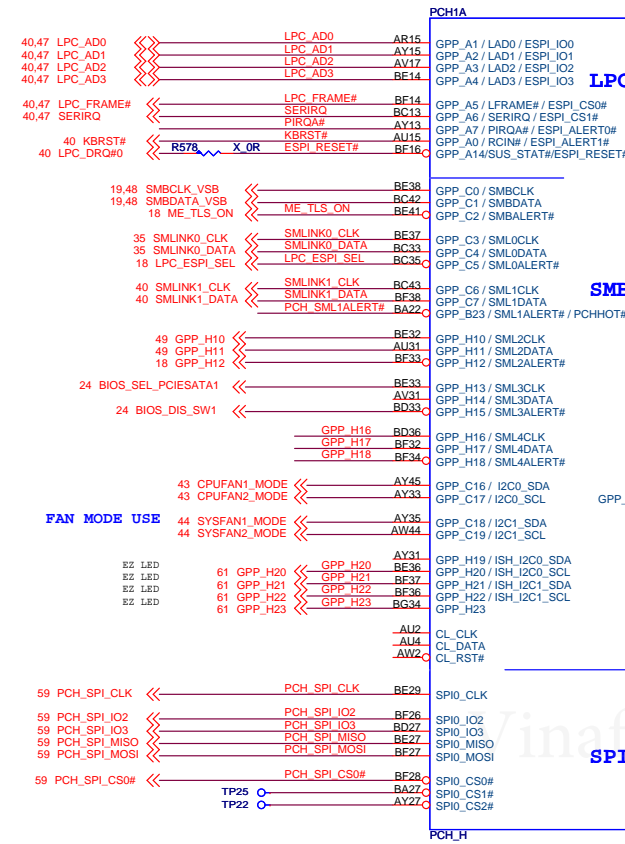
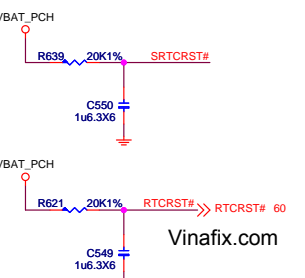


PCH GPIO For BIOS DETCET MSI ID USED

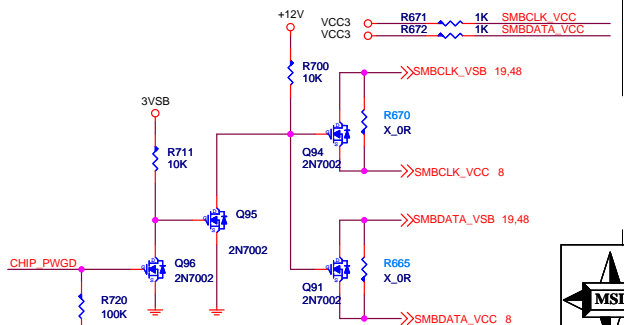
Chassis Intrusion



RTC



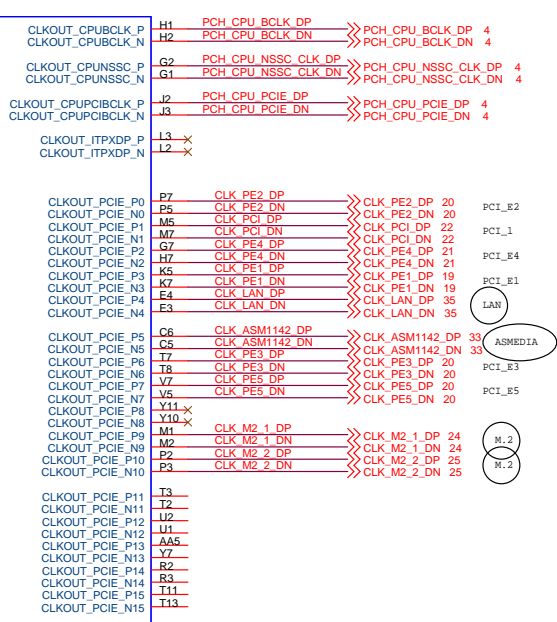
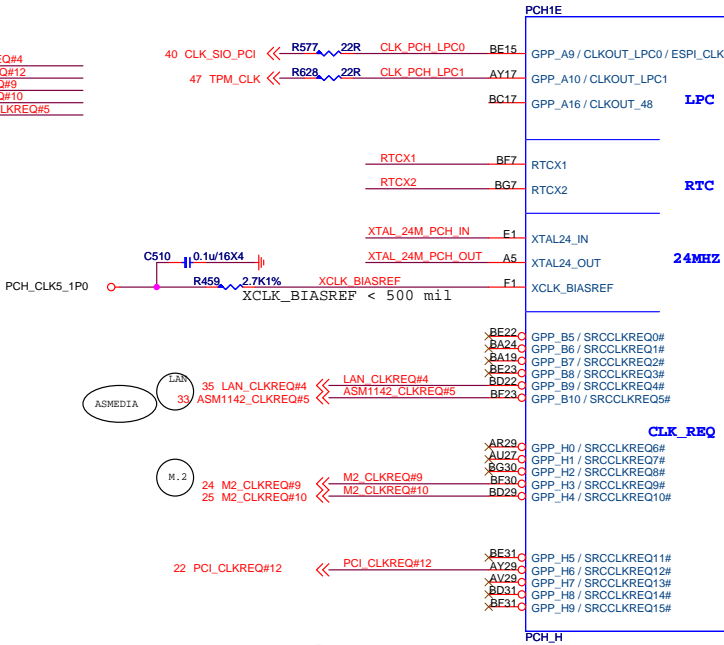
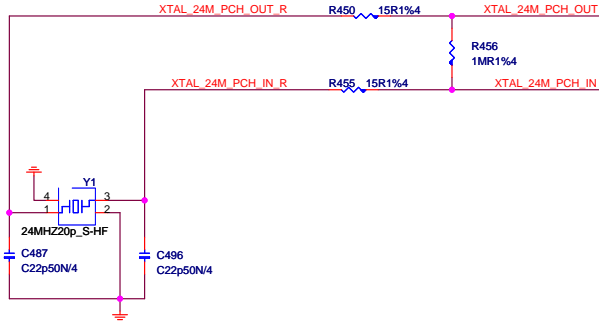
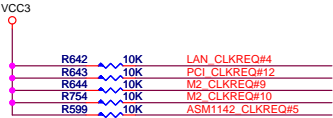
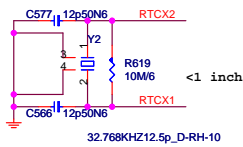
擺在一起 (注意到所有的SMBUS的分枝)



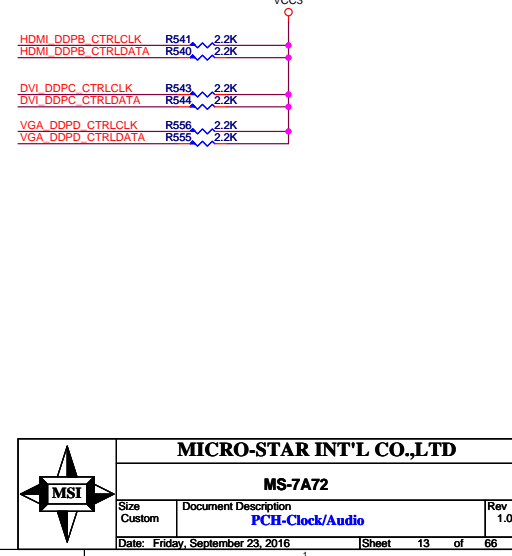
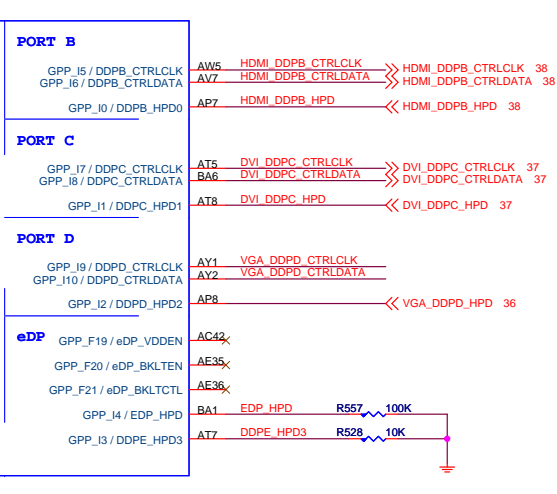
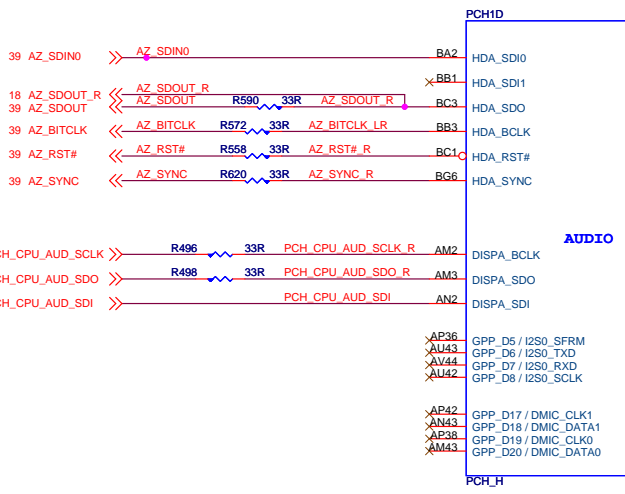
PCH_CLK

RTC Block


Close to PCH



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MS-7A72

Size Custom

Document Description

PCH-Clock/Audio

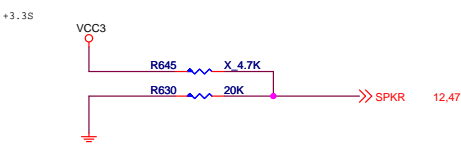
Date: Friday, September 23, 2016

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Rev 1.0

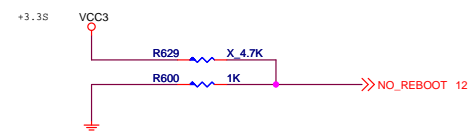
VSS

TOP Swap



Internal pull-down is disabled after PLTRST#

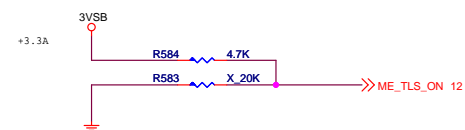
No Reboot



- 0 : DISABLE (Default)
- 1 : ENABLE

Internal pull-down is disabled after PLTRST#

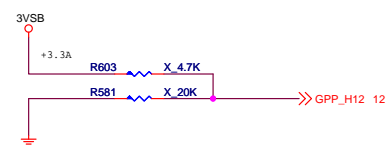
AMT and SBA with confidentiality



- 0 : DISABLE
- 1 : ENABLE (Default)

Internal pull-down is disabled after RSMRST

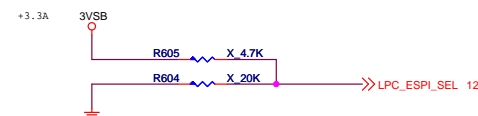
ESPI FLASH SHARING MODE



- 0 : MASTER ATTACHED FLASH SHARING
- 1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down is disabled after RSMRST

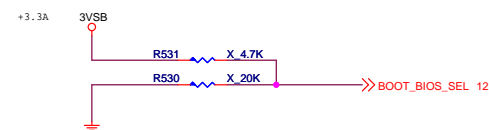
LPC eSPI Mode



- 0 : LPC
- 1 : eSPI

Internal pull-down is disabled after RSMRST

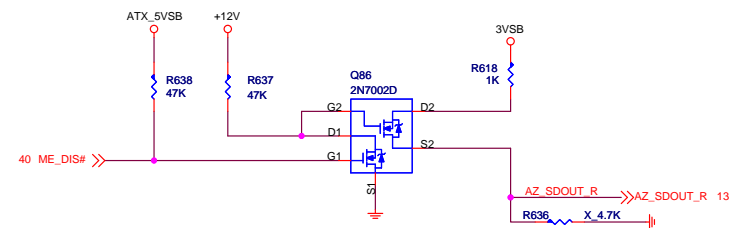
Boot BIOS



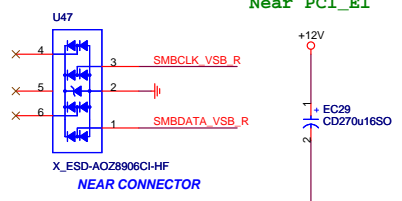
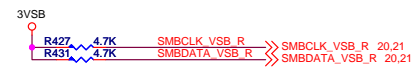
- 0 : SPI
- 1 : LPC

Internal pull-down is disabled after PLTRST

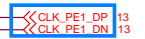
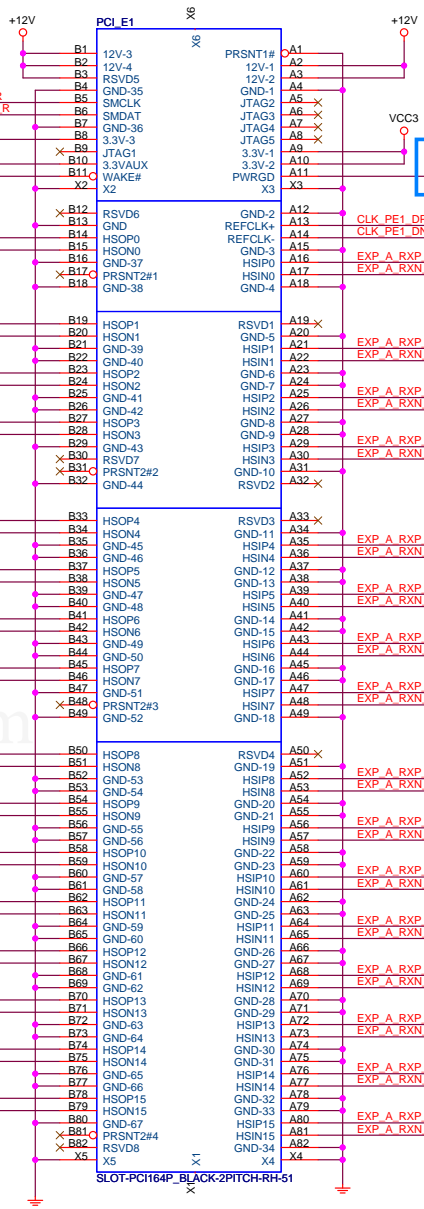
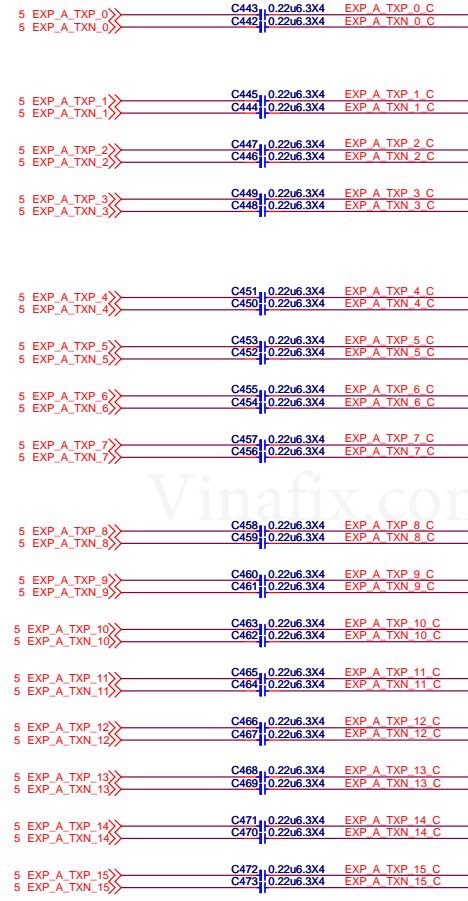
HDA_SDO



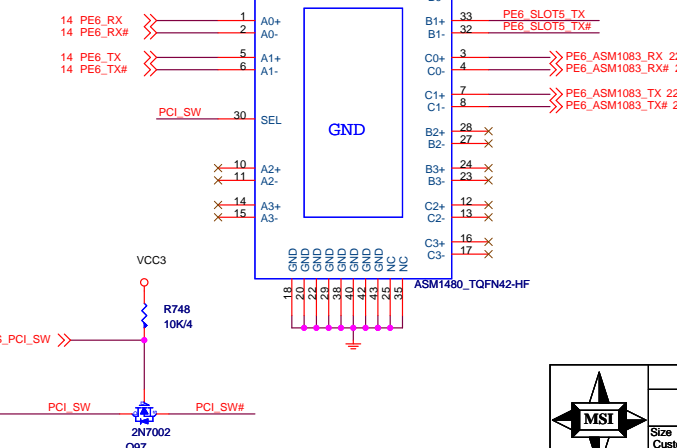
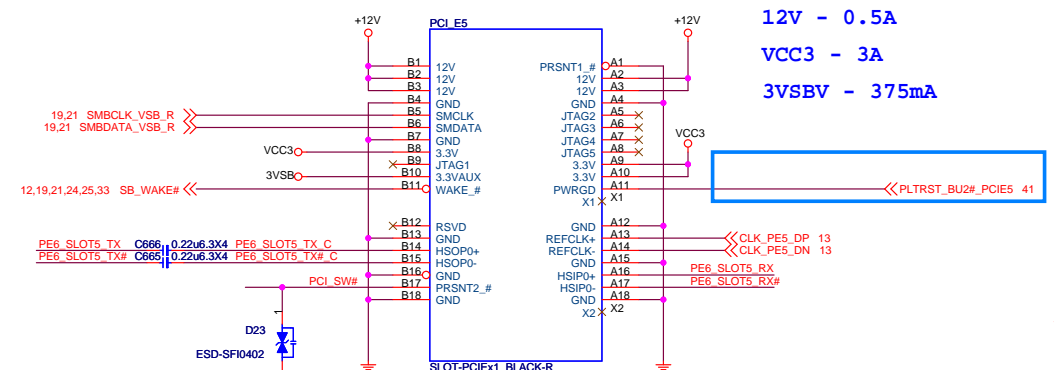
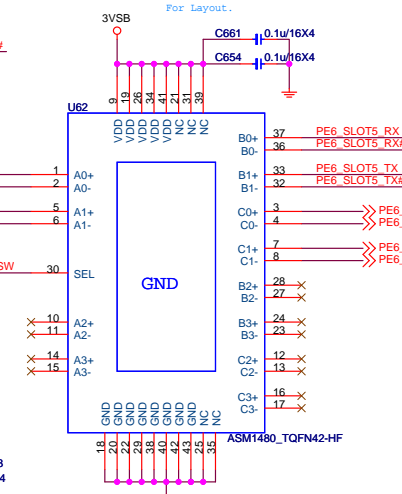
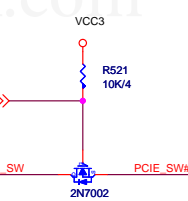
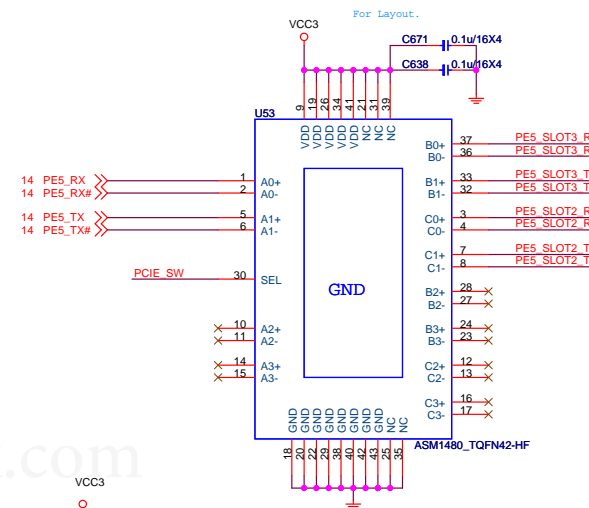
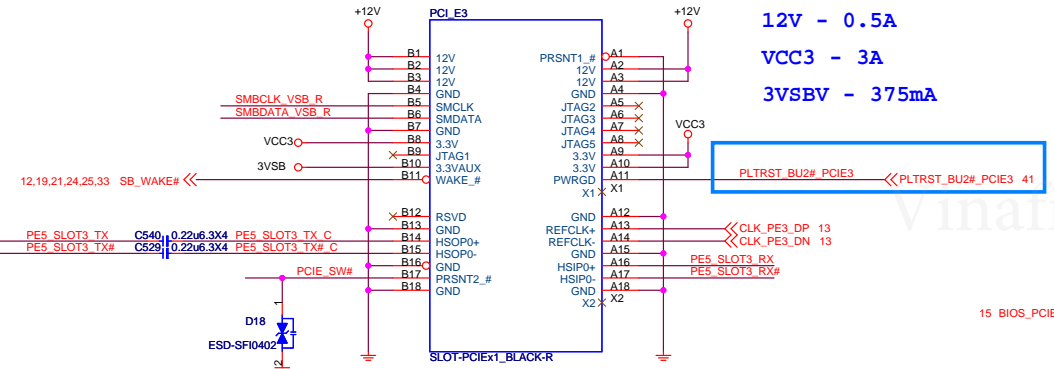
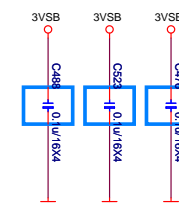
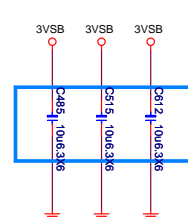
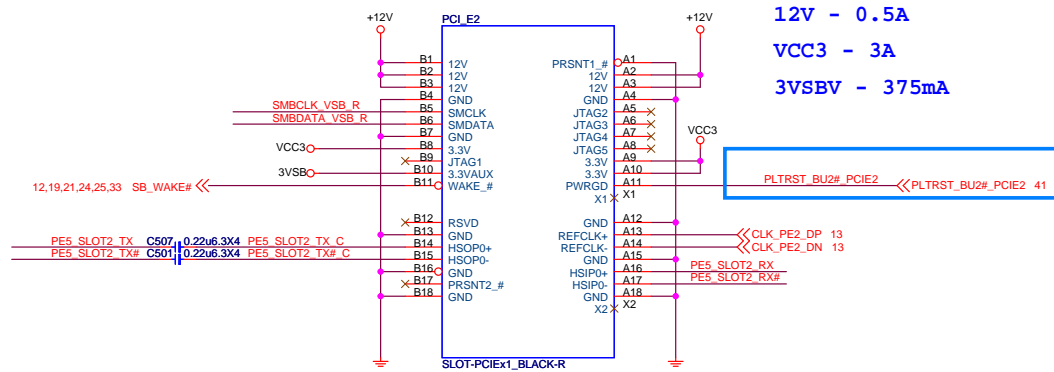
12V - 5.5A
VCC3 - 3A
3VSBV - 375mA



12,20,21,24,25,33 SB_WAKE#



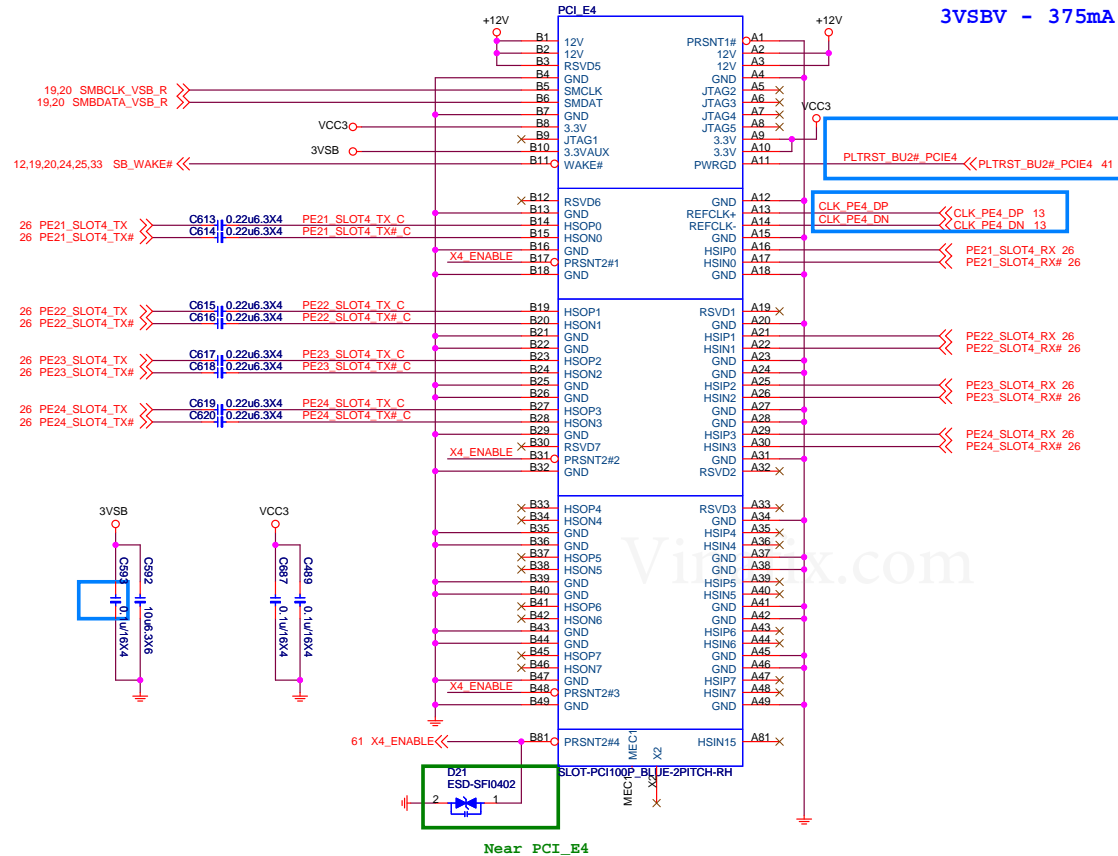
Vinafix.com



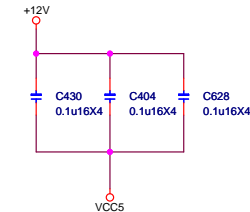
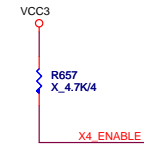
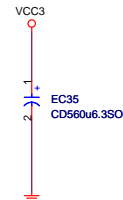
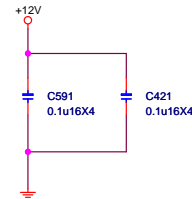
Vinafix.com

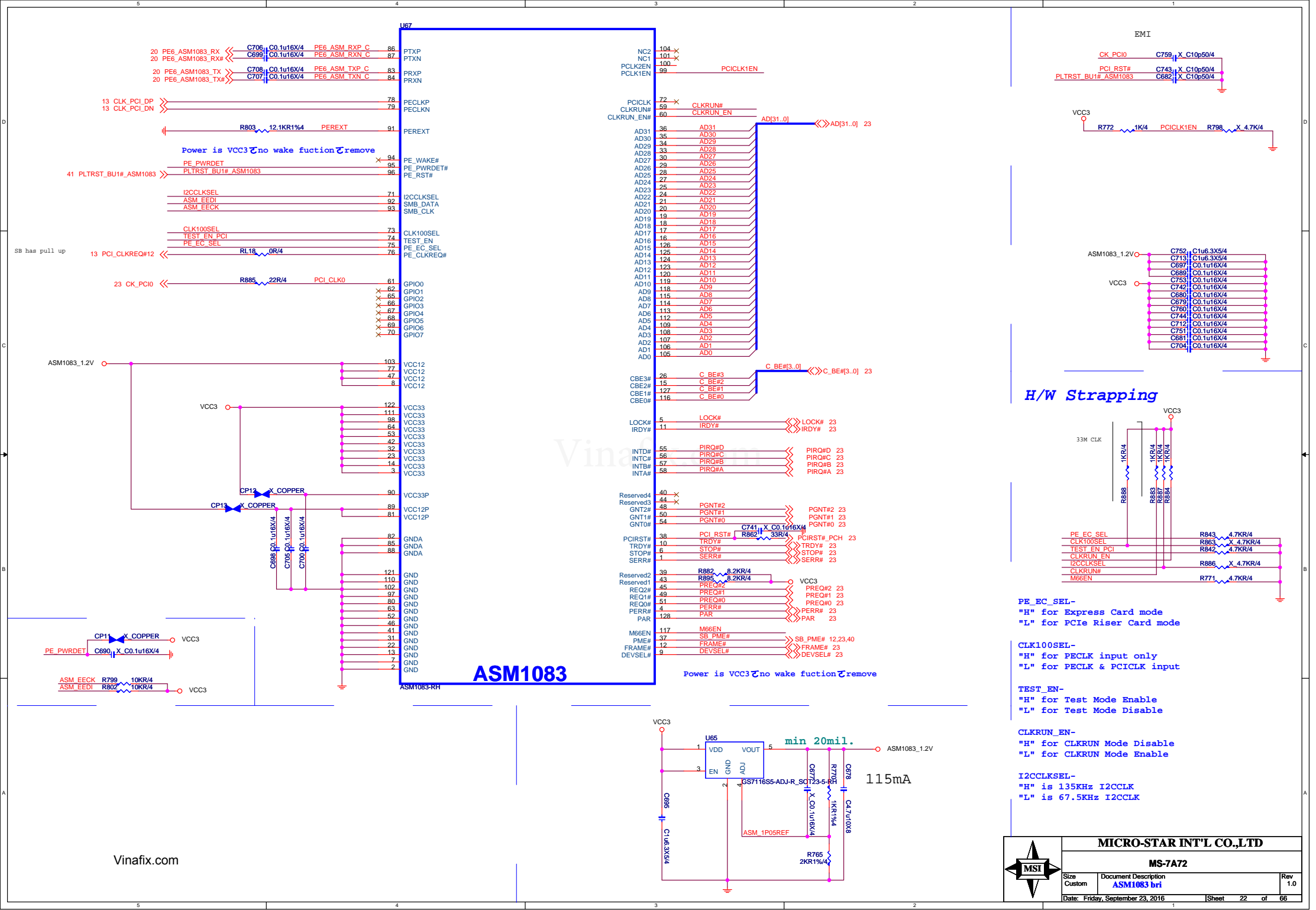
PCI_Express X4 slot

12V - 2.1A
VCC3 - 3A
3VSBV - 375mA



Near PCI_E4

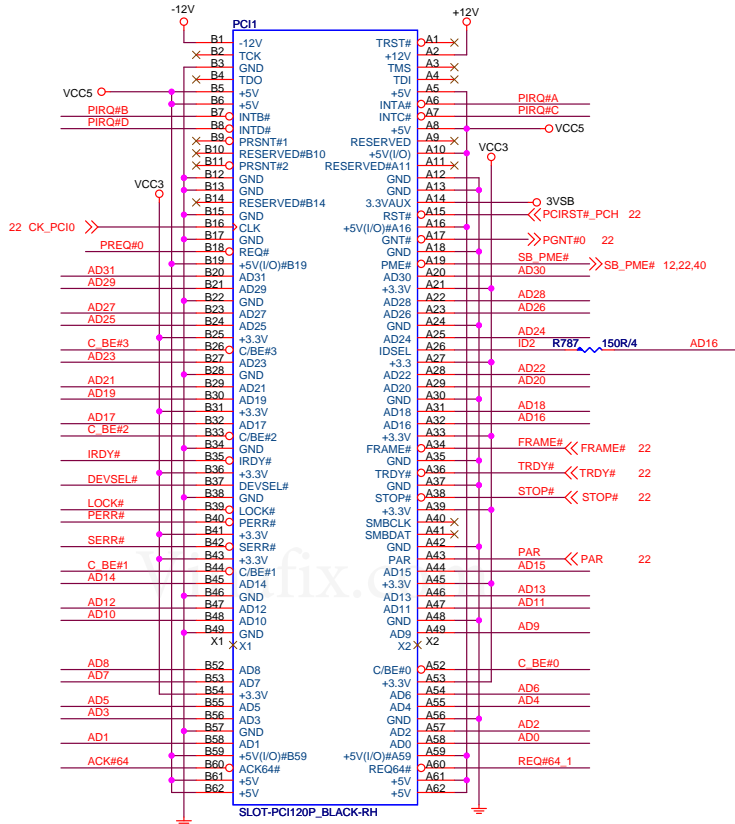




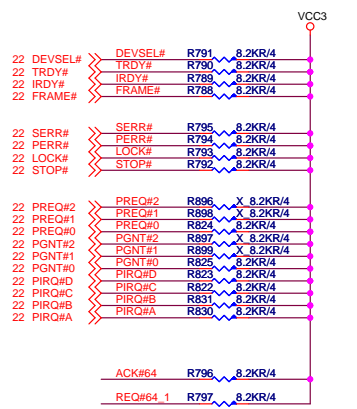
PCI

3.3Vaux:0.375*2=0.75A(wake)
0.02*2=0.04A(no wake)
VCC3 :7.6*2=15.2A
VCC5:5*2=10A
+12V:0.5*2=1A
-12V:0.1*2=0.2A

AD[31..0] <<<> AD[31..0] 22
C_BE#[3..0] <<<> C_BE#[3..0] 22

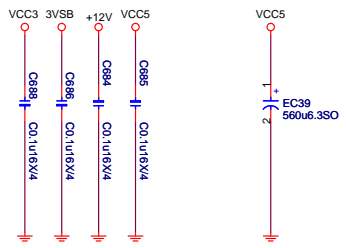


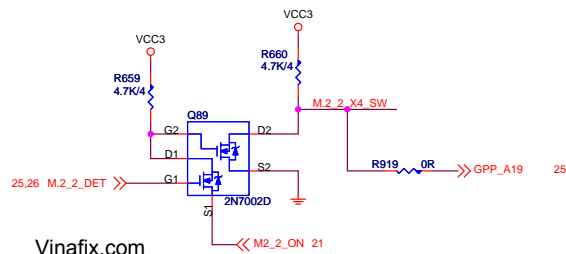
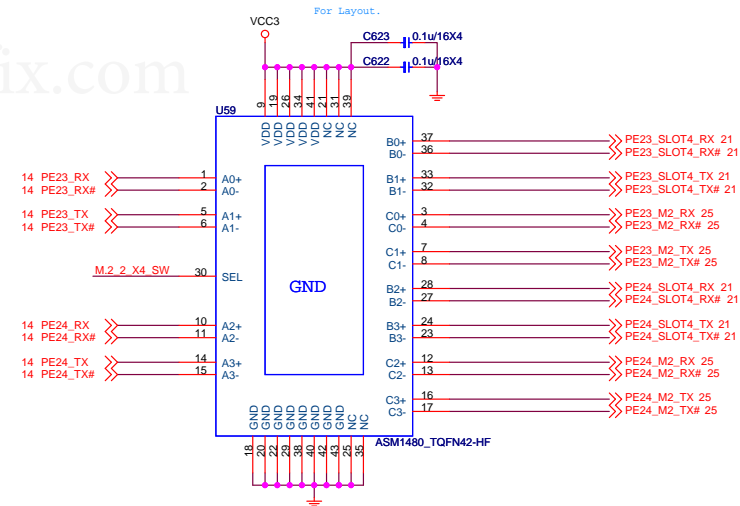
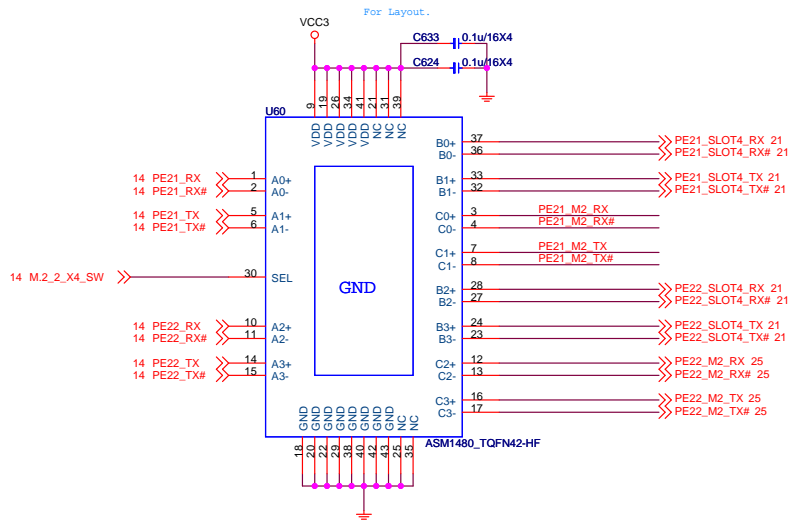
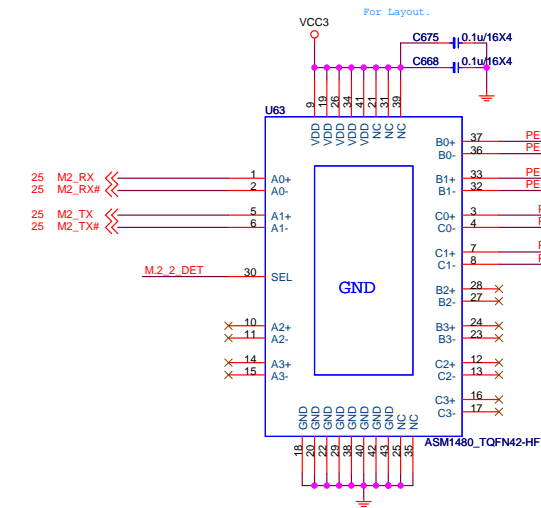
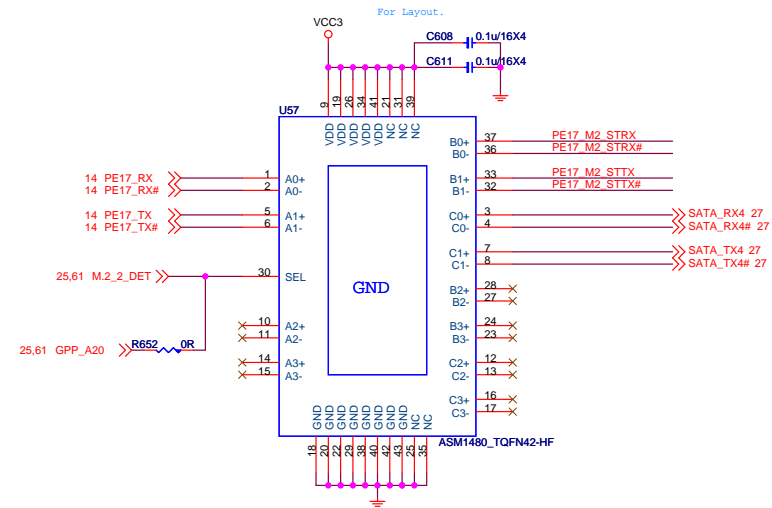
PCI PULL-UP / DOWN RESISTORS



IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

EMI:close pin





Default

M.2_2 PCIE

M.2_2 SATA

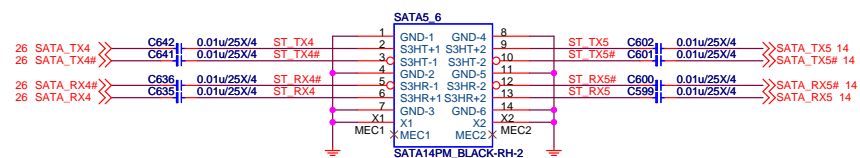
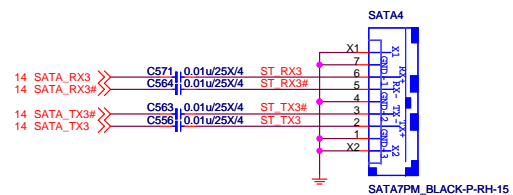
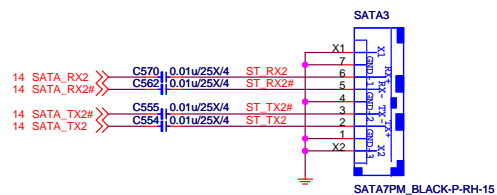
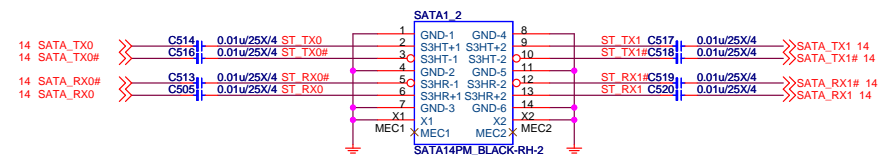
| M.2_2_ON | M.2_2_X4_SW | M.2 SATA | M.2 PCIE | X4 SLOT | SATA5 |
|----------|-------------|----------|----------|---------|-------|
| V | V | X | X | V | V |
| X | X | X | V | X | V |
| X | V | V | X | V | X |



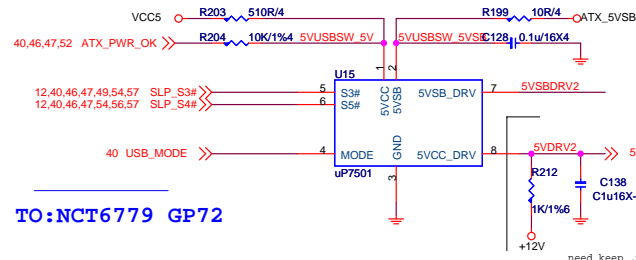
MICRO-STAR INT'L CO.,LTD

MS-7A72

| Size | Document Description | Rev |
|----------------------------------|----------------------|-----|
| Custom | M.2/SATA/PCIE SW | 1.0 |
| Date: Friday, September 23, 2016 | Sheet 26 of 66 | |



REAR USB PORT POWER

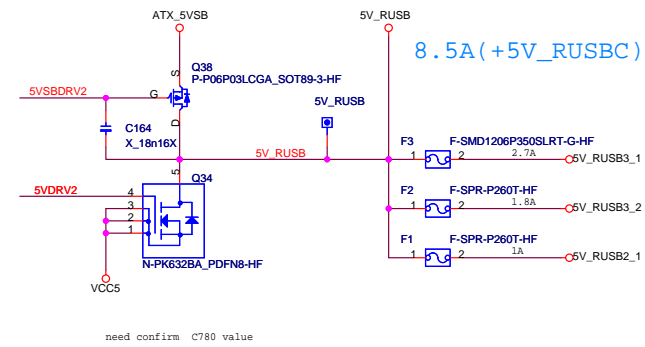


TO:NCT6779 GP72

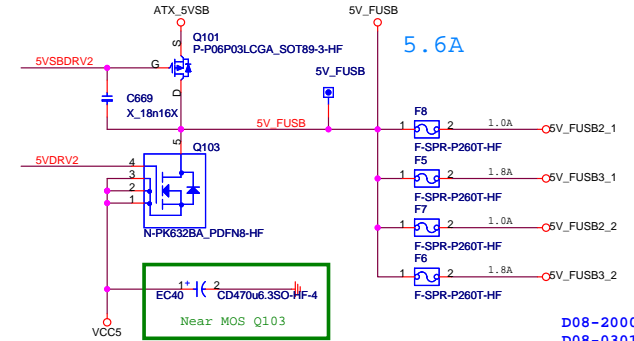
H:SUPPORT S0/S3/S5
L:SUPPORT S0/S3

5VDRV2, 5VSBDRV2 width 12mil,
Do NOT route near the edge of a board.

need keep .when using SIO control



need confirm C780 value

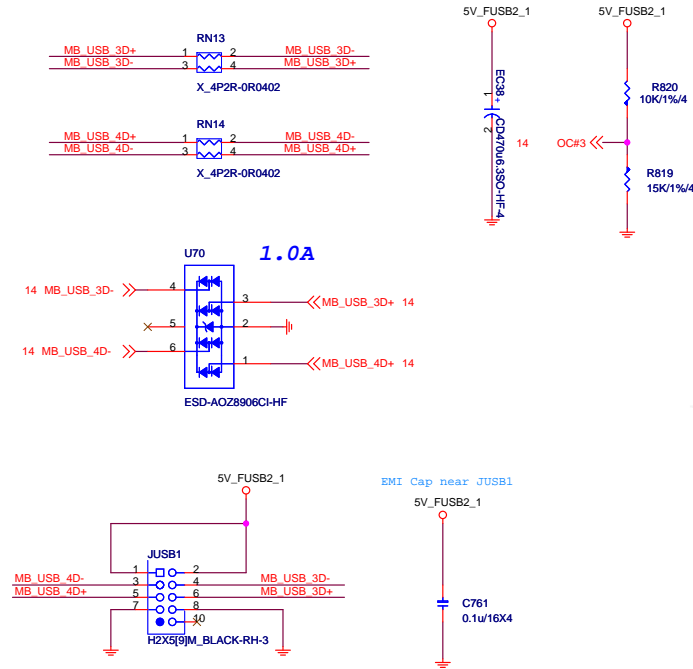


P-MOS
D03-06P0319-N03

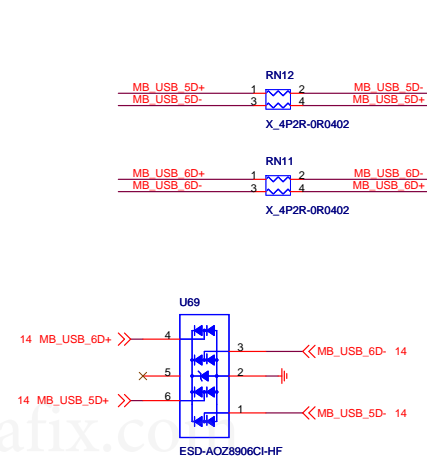
N-MOS
D03-510BA0C-N03
D03-3056M00-U47
D03-4C05N03-O05
D03-3830D09-N47
D03-632BA0C-N03

D08-2000400-P16 (Itrip=3.5A; 0.003ohm)
D08-0301000-P16 (Itrip=2.6A; 0.015ohm)

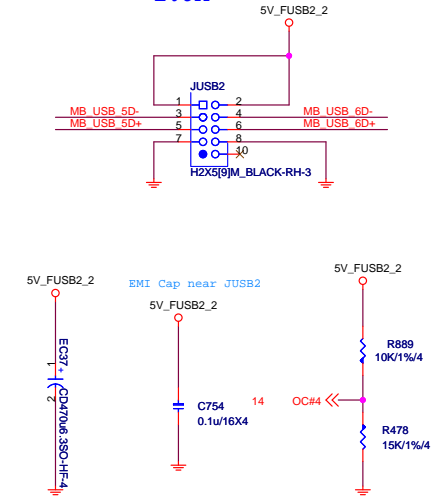
FRONT USB2.0 PORT 3,4

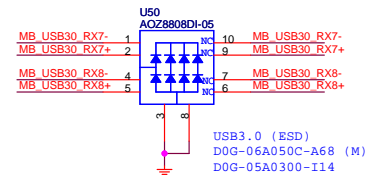
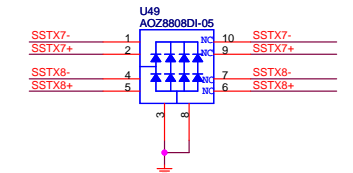
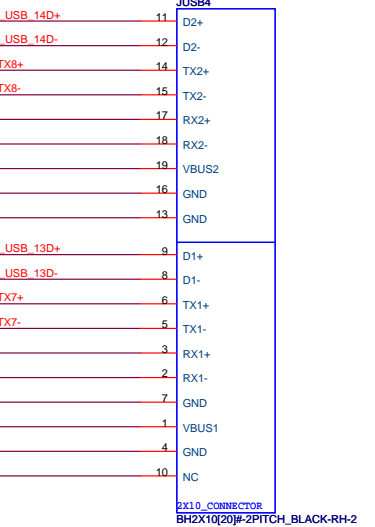
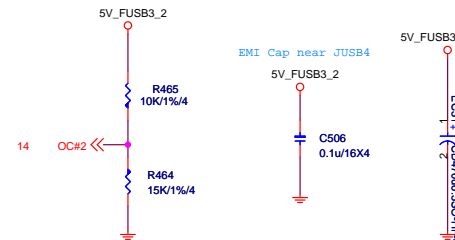
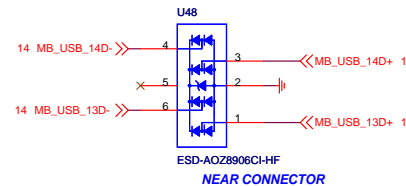
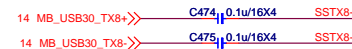
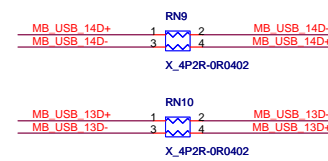
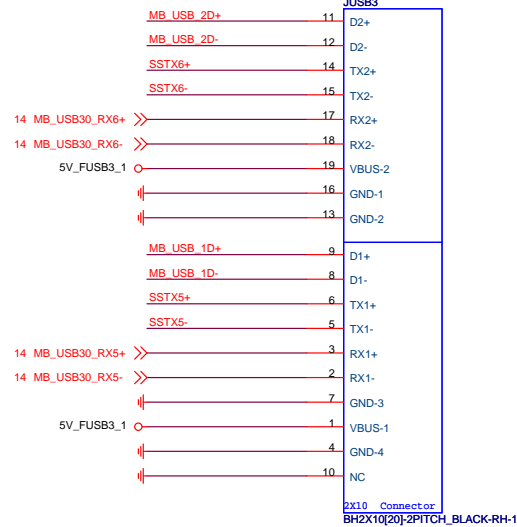
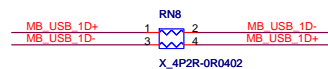
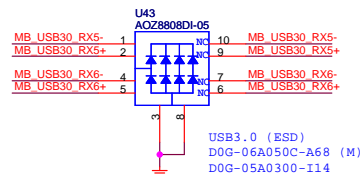
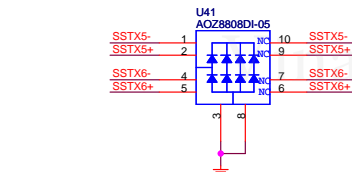
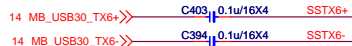
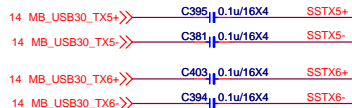
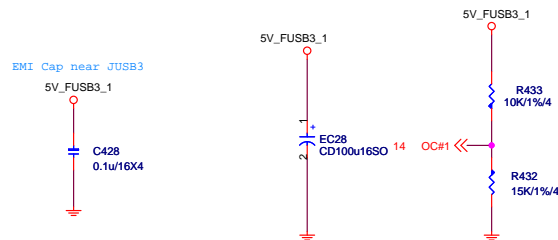
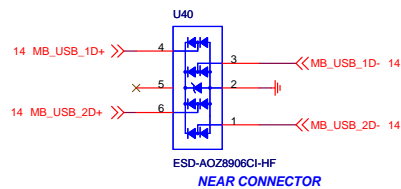


FRONT USB2.0 PORT 5,6



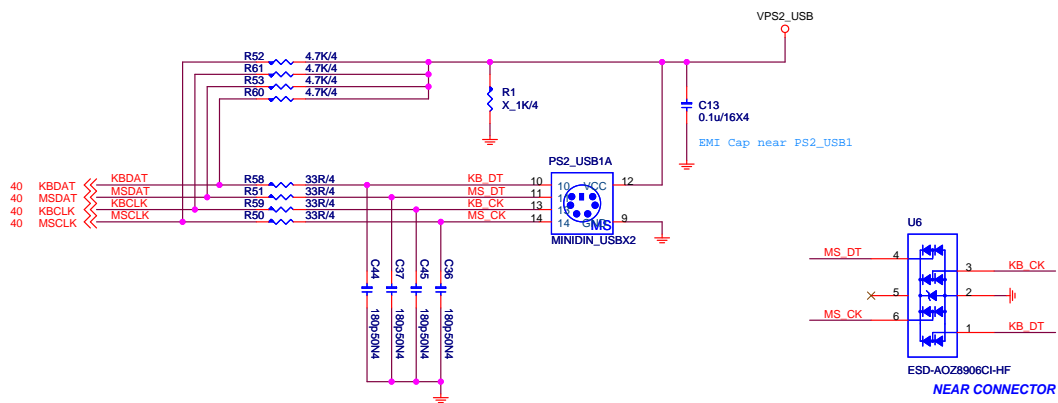
1.0A



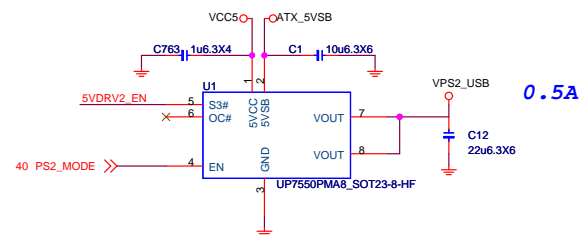


PS2 KEYBOARD & MOUSE CONNECTOR

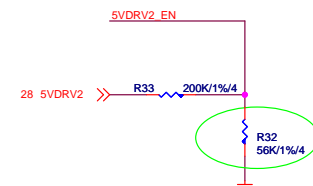
PS2 Connector



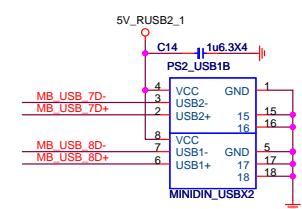
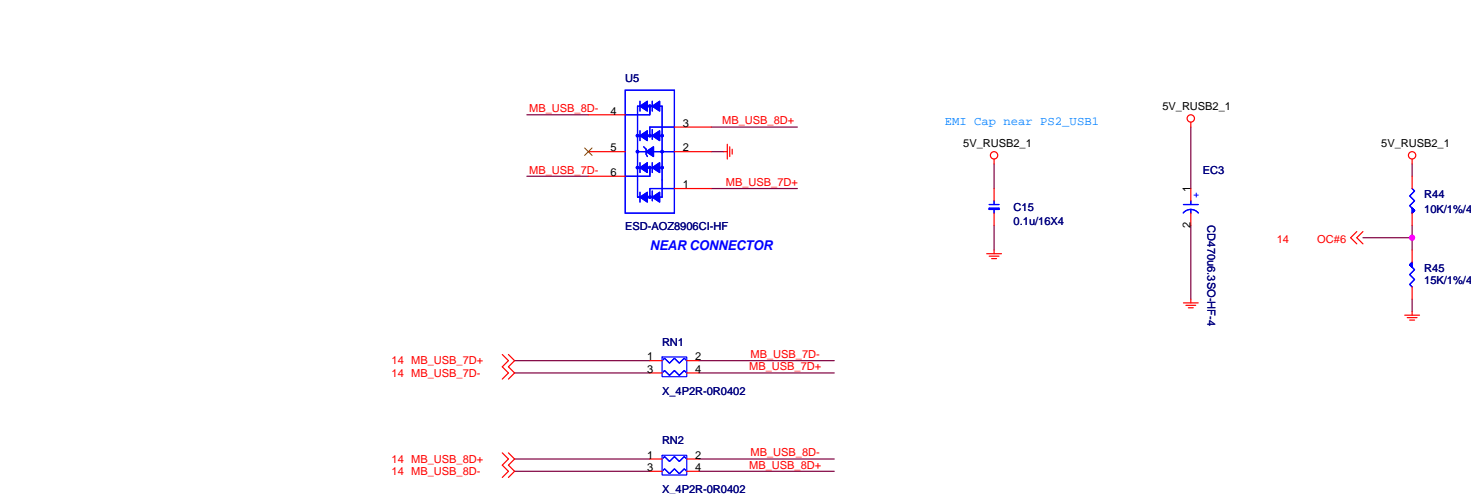
PS2 Power

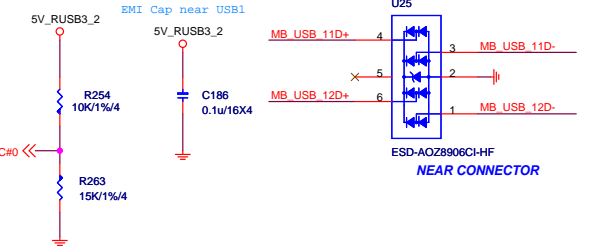
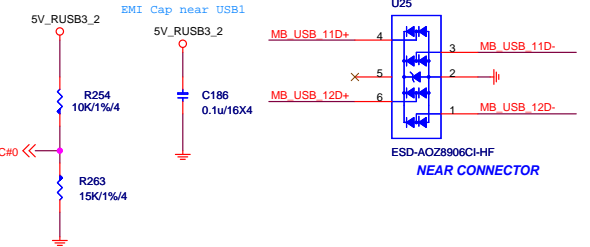
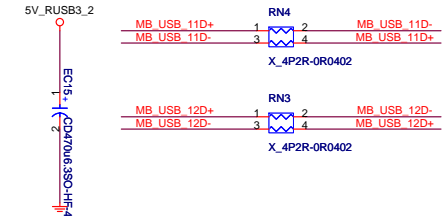
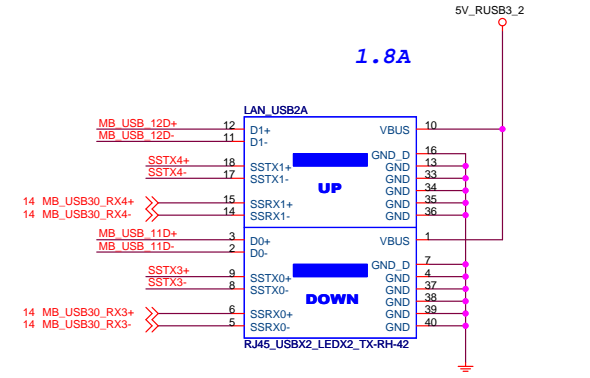
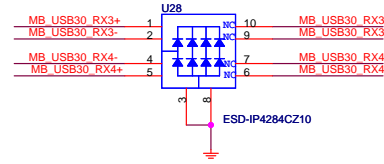
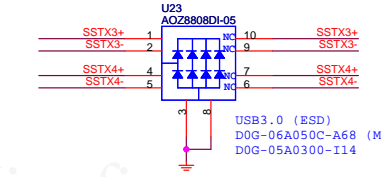
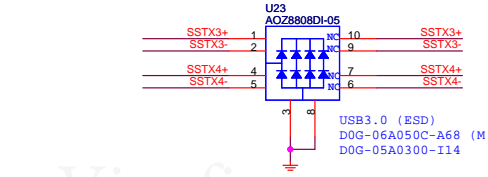
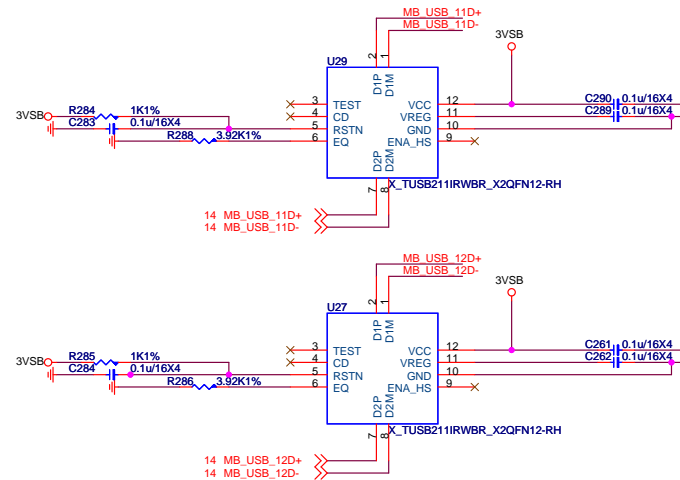
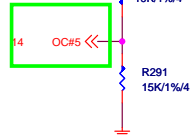
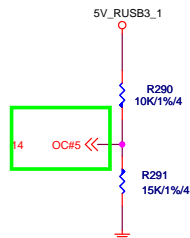
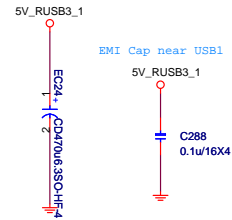
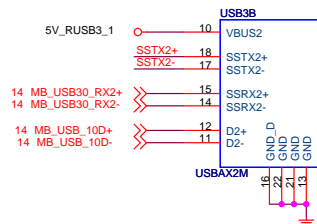
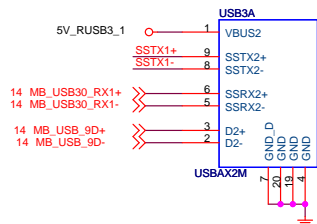
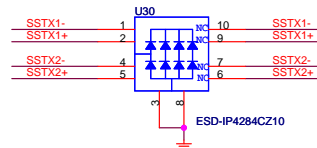
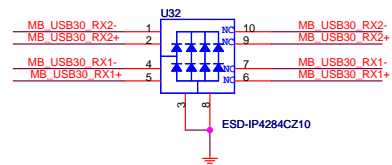
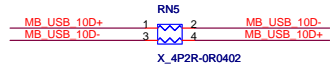
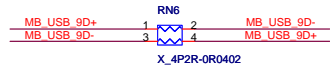
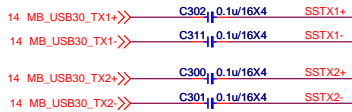
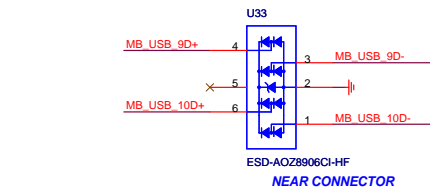


USB MODE

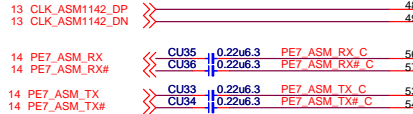


PS2_USB

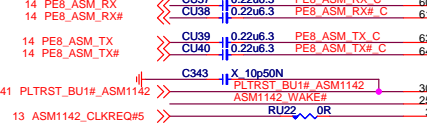




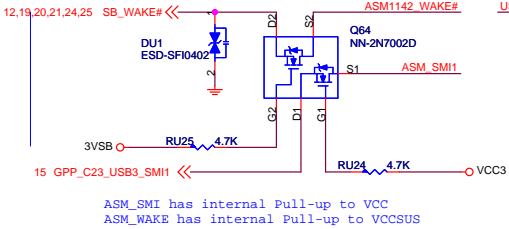
CLK Rule (Follow SB PDG)



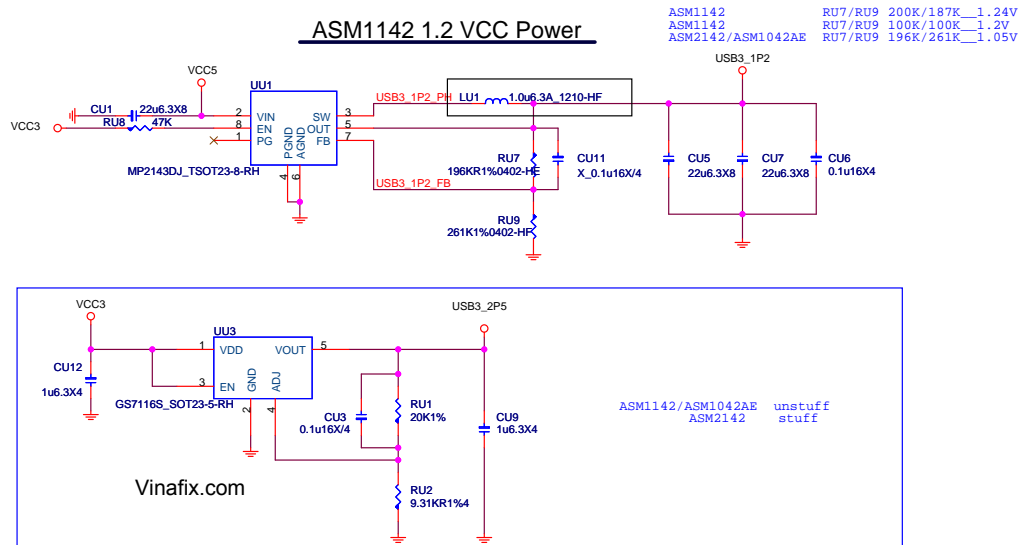
PCIE Rule (Follow SB PDG)



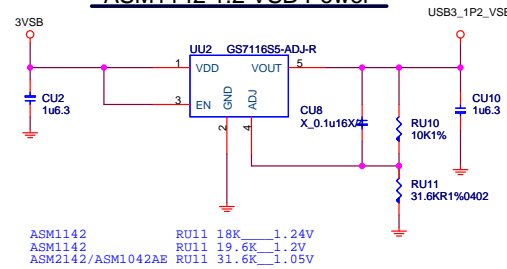
SMI connect to GPI which support smi function.
SB side pull high 10K ohm to 3VSB.
(Intel 8X & 9X series use GPIO10)
(Intel SKL use GPP_C23)



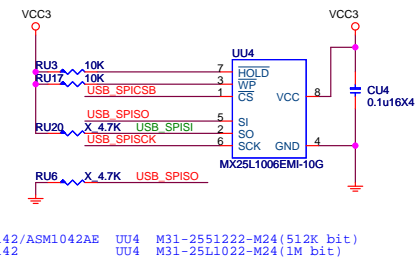
ASM1142 1.2 VCC Power



ASM1142 1.2 VSB Power



EEPROM



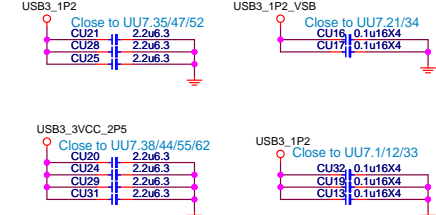
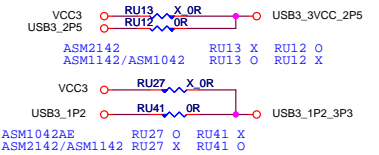
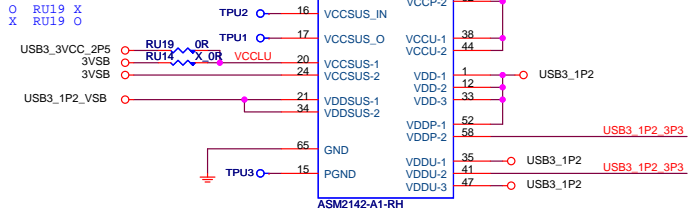
Power Consumption

| | 3.3V | 1.2V(1.05V) | 3.3VSUS | 1.05VSUS(1.2VSUS) | 2.5V | Total Power |
|---------|-------|-------------|---------|-------------------|------------|-------------|
| ASM1142 | 245mA | 634mA | 1mA | 1mA | | 1573.8(mW) |
| ASM2142 | TDP | TDP | TDP | TDP | 300mA(TDP) | TDP |

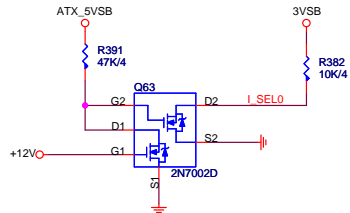
Layout Guide:

- 1.) USB3.1 to Connector Total Length < 1.5"
- 2.) VIA hole < 2

ASM1142/ASM1042 RU14 O RU19 X
ASM2142 RU14 X RU19 O



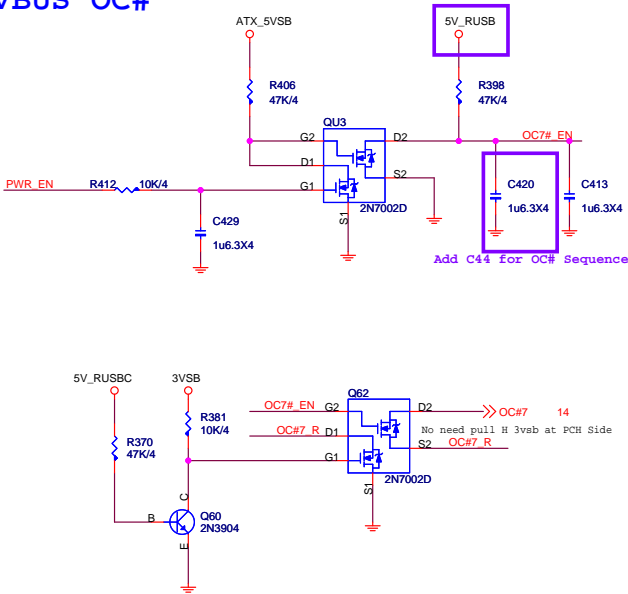
Current Mode



| | |
|---------------|-------------------|
| I_SELO:I_SEL1 | |
| X 0 | Default for 900mA |
| 0 1 | 1.5A @5V |
| 1 1 | 3A @5V |

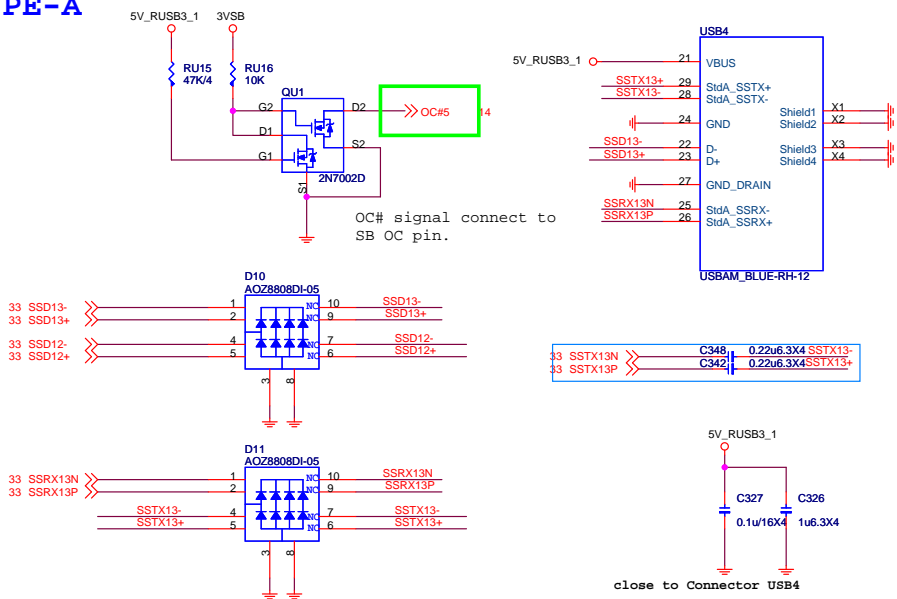
1.5A under S3 mode
3A under S0 mode

VBUS OC#



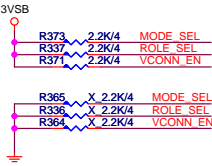
Add C44 for OC# Sequence

TYPE-A



OC# signal connect to SB OC pin.

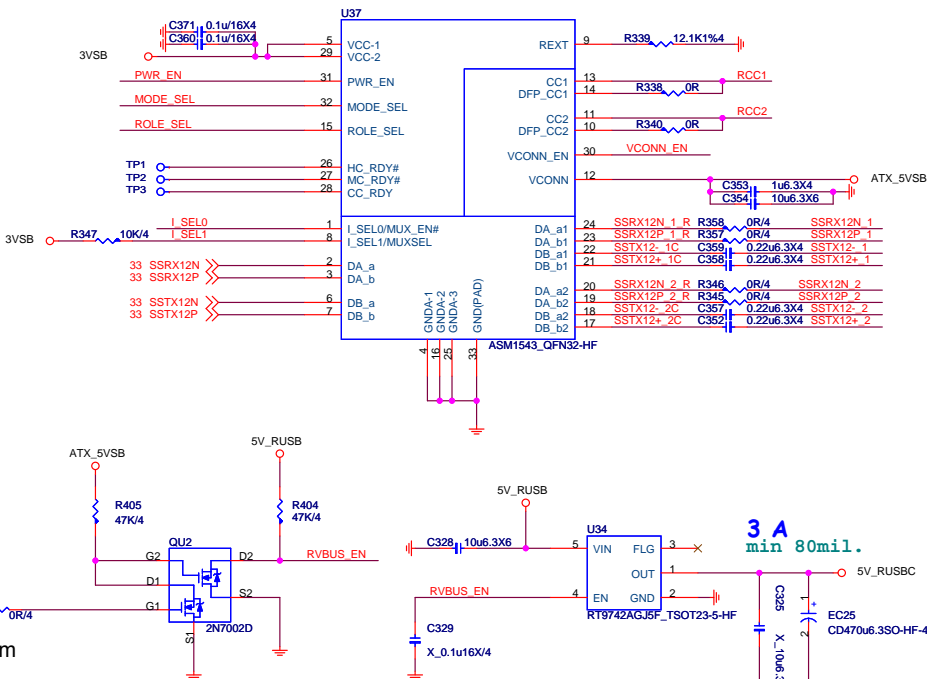
USB Type-C MUX with Configuration Channel (CC)



| MODE_SEL | |
|----------|--------------------|
| 1 | CCL MODE (default) |
| 0 | Mux MODE |

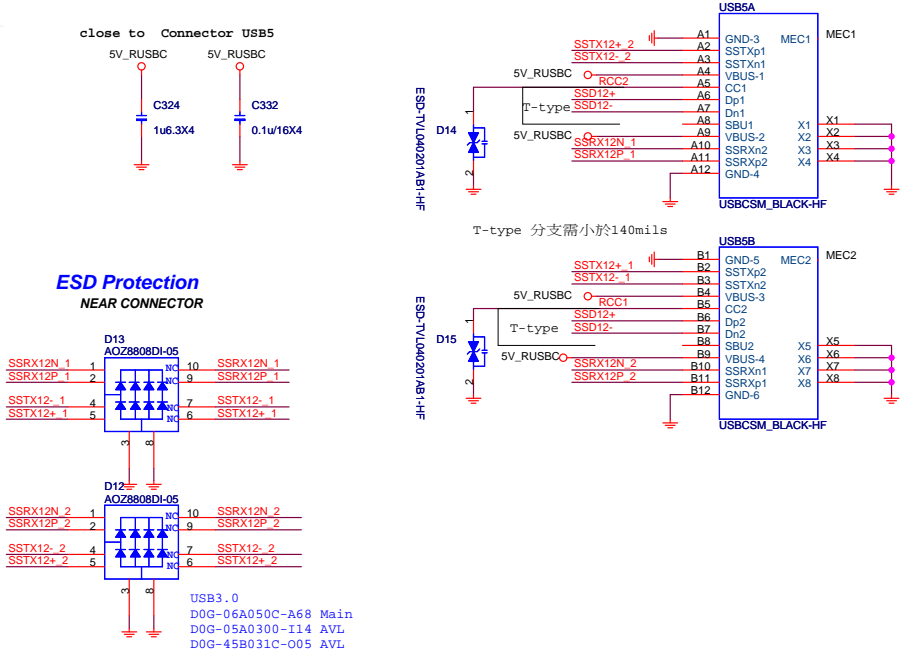
| ROLE_SEL | |
|----------|--------------------|
| 1 | DFP role (default) |
| 0 | UFP role |

| VCONN_EN | |
|----------|---------|
| 1 | enable |
| 0 | disable |



3 A min 80mil.

TYPE-C

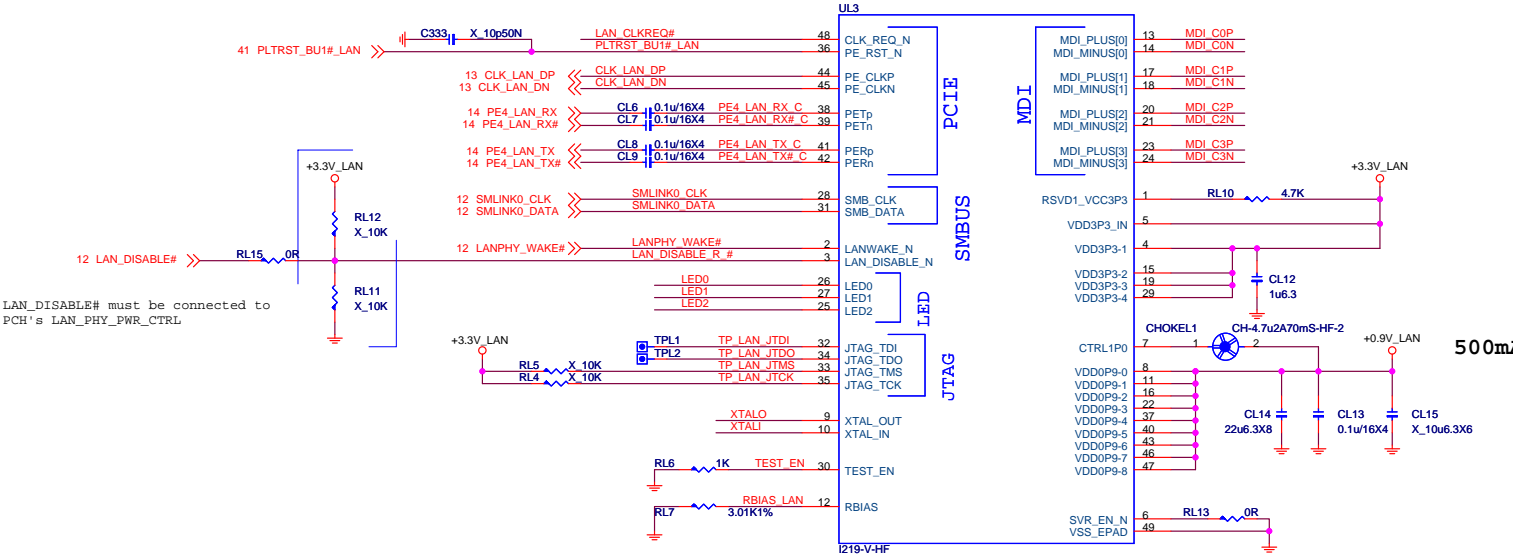


ESD Protection
NEAR CONNECTOR

USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL
D0G-45B031C-005 AVL

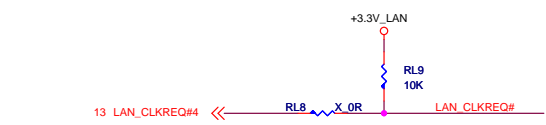
Intel Lan- I219

8111H:B06-08111CC-R09
8111G:B06-081116C-R09



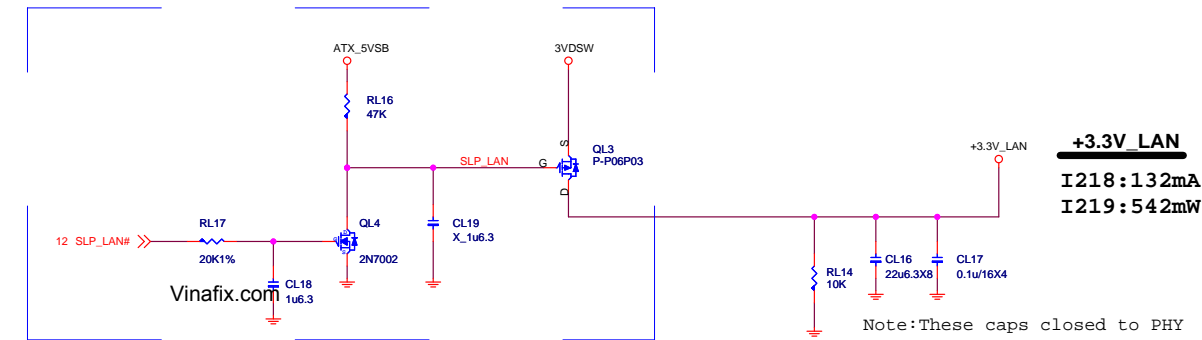
LAN_DISABLE# must be connected to PCH's LAN_PHY_PWR_CTRL

PCH's PCIECLKRQ<n> port must be mapped to PCH's PET/R<n+1>port. If CLK_REQ_N is not used, pin48 is pulled up 10KR to 3.3V_LAN



The 10Kohm pull-up resistor (RL18) of CLK_REQ_N is connected to 3.3V Suspend/Core/etc. power well, depending on the power well of PCH's input PCIECLKRQ<n> buffer.

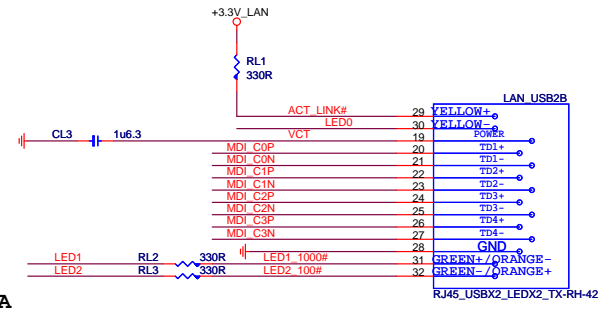
support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.



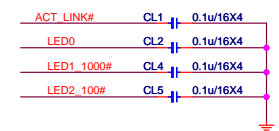
Note: These caps closed to PHY

+3.3V_LAN
I218: 132mA
I219: 542mW

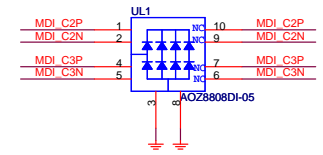
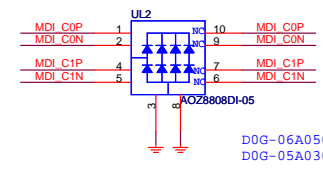
LAN Connector



For EMI



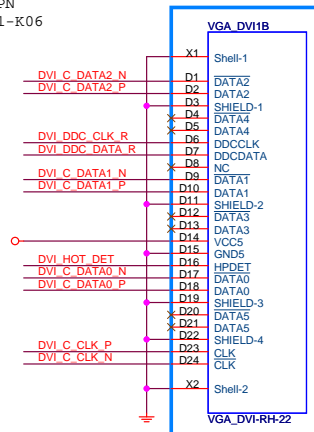
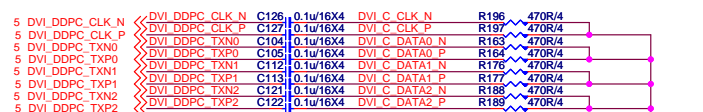
UL2&UL3 close to connector



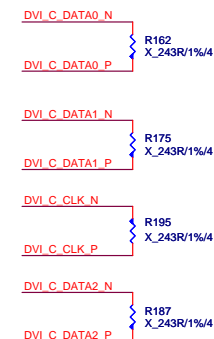
Do not pair MDI0 and MDI1 on the same TVS device (avoid LAN POE connecting issue). Other pairing combination is ok.

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

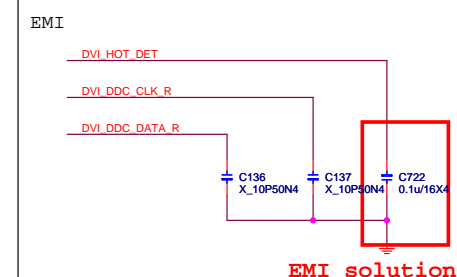
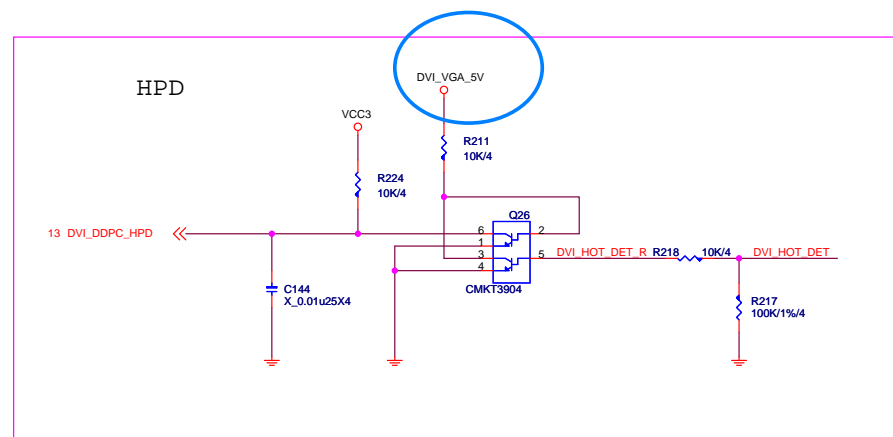
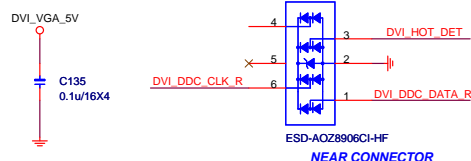
Check MSI PN
N58-39F0231-K06



For EMI

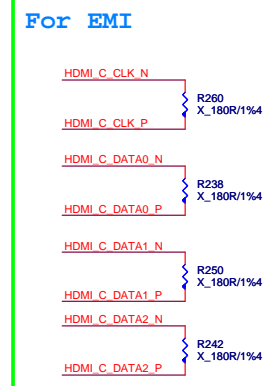
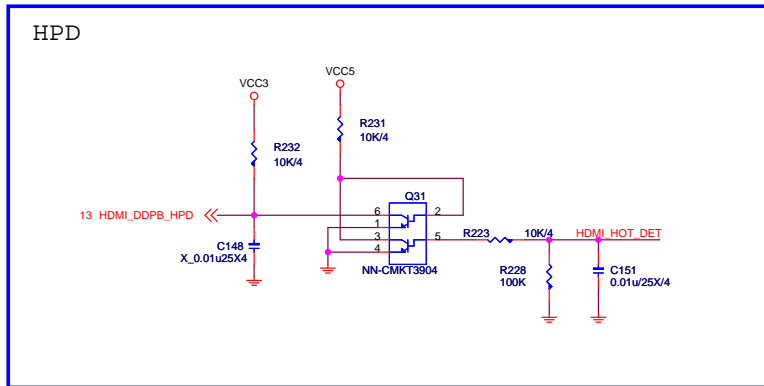
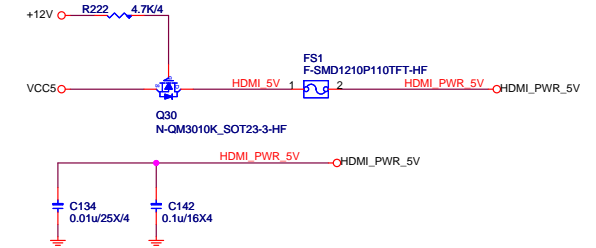
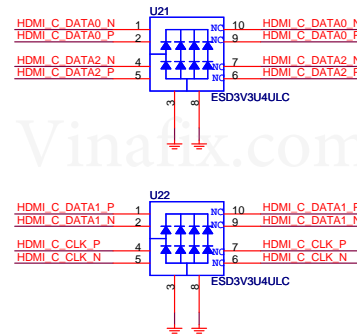
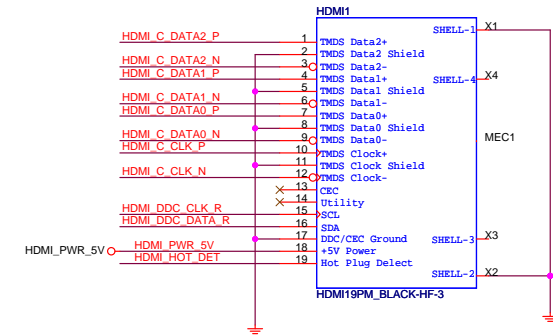
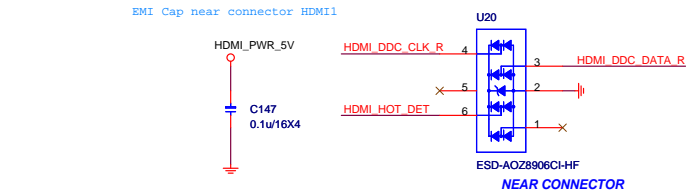
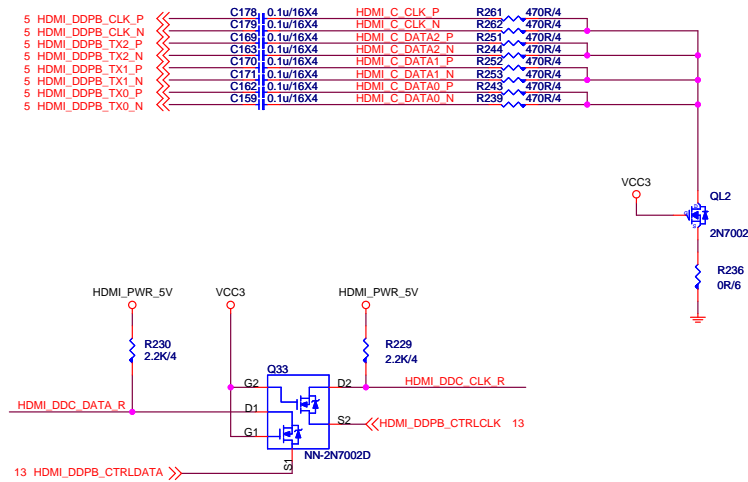


EMI Cap near connector DVI1

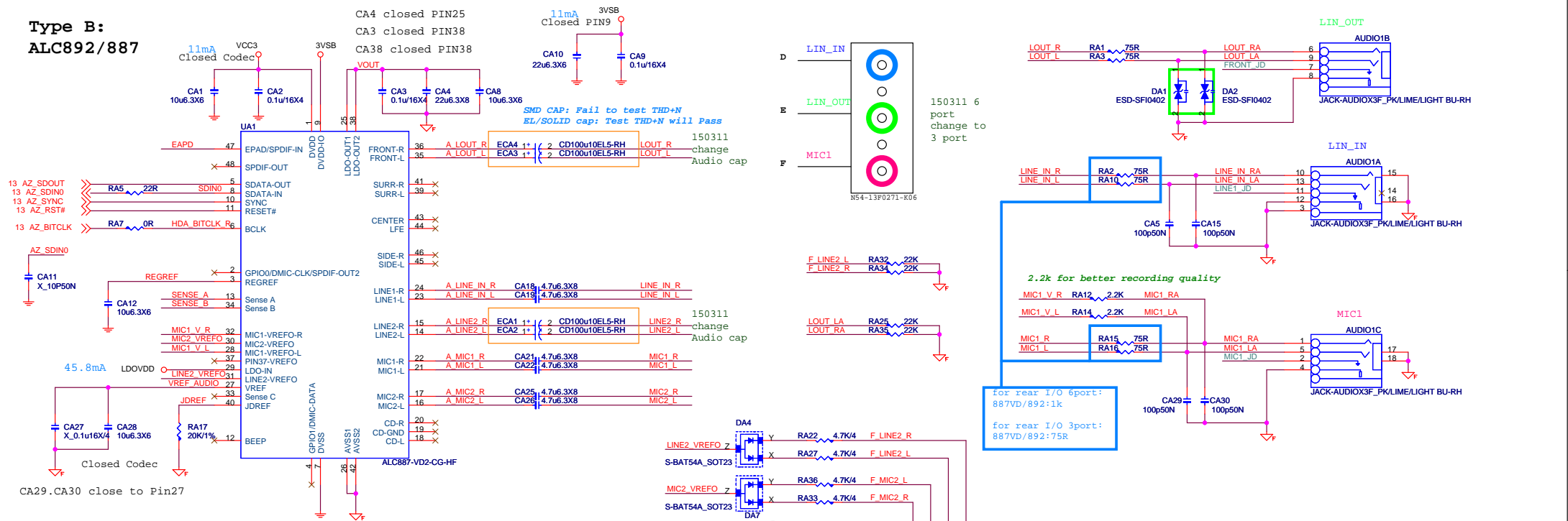


Vinafix.com

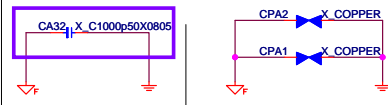
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



Type B: ALC892/887

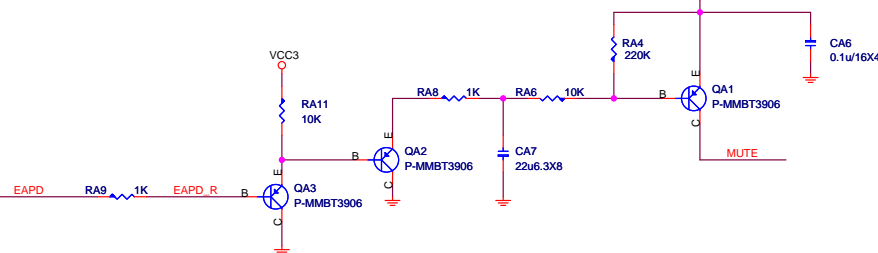


EMI 移除电容且换package0805



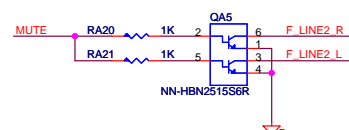
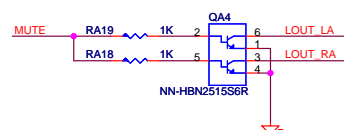
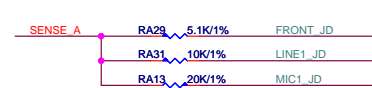
Rear Line OUT De-POP circuit

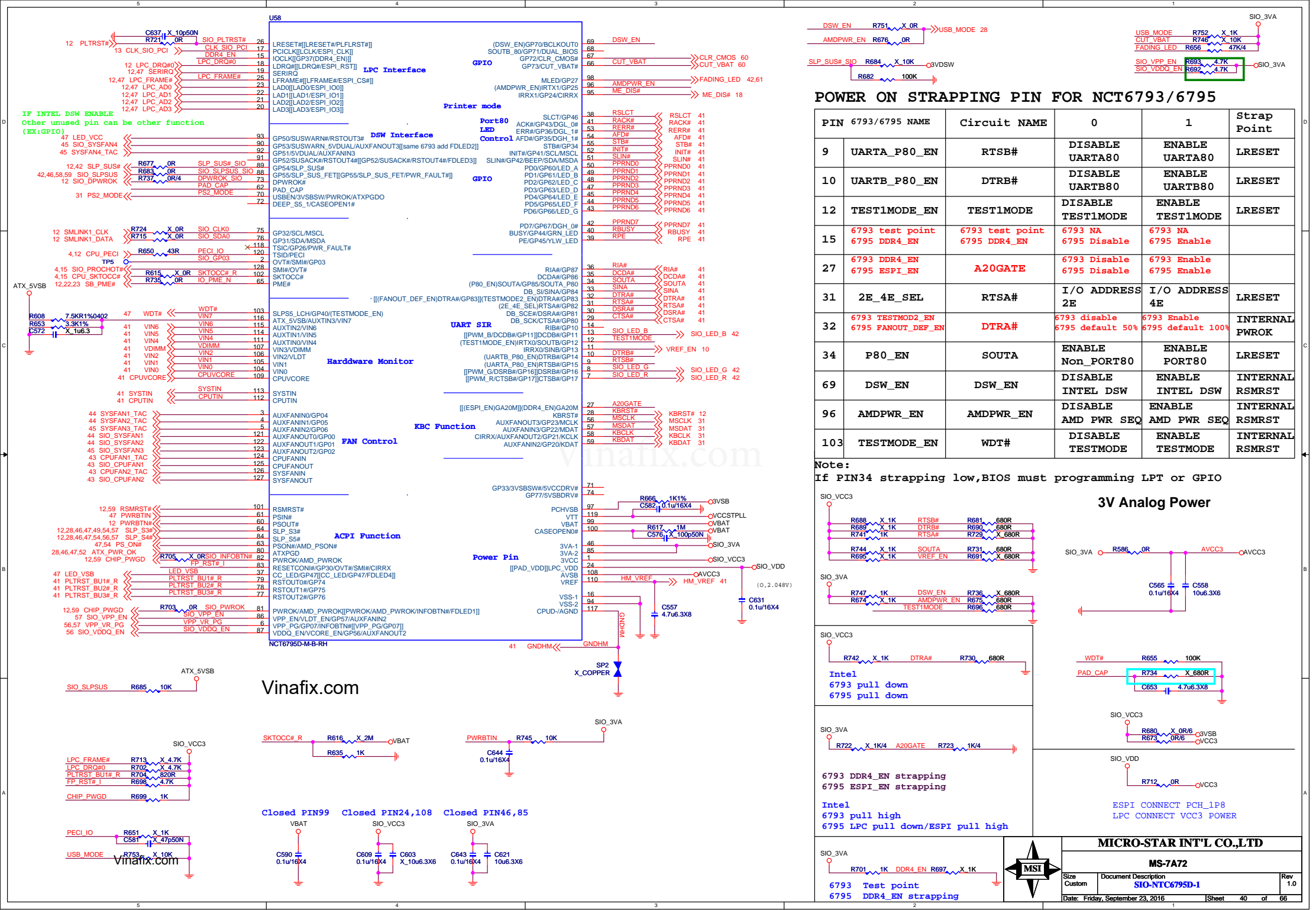
De-pop circuit for Rear Line out & Front Headphone out)



Digital

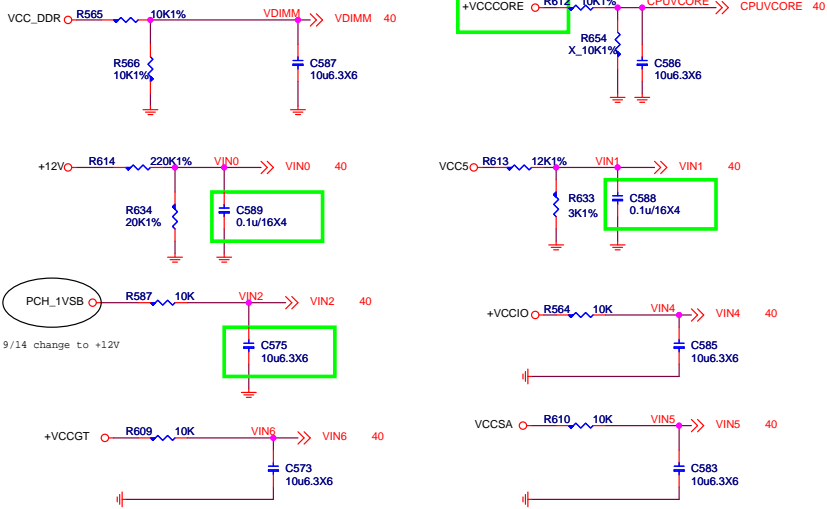
Analog



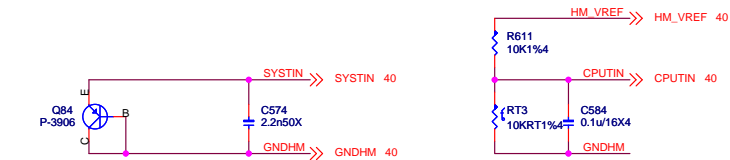


HW Monitor - Voltage

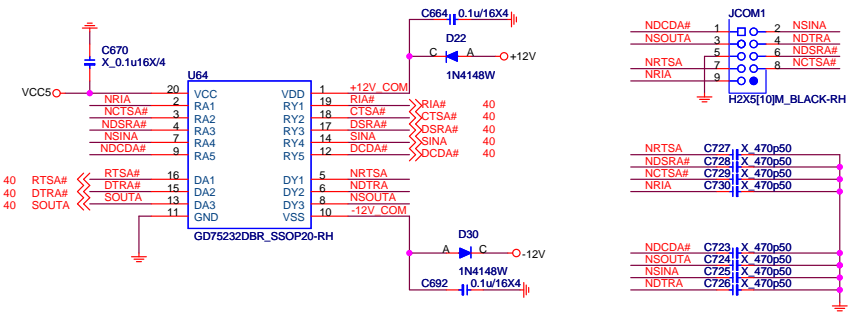
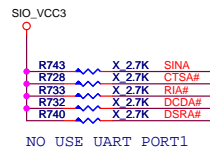
SIO HM Voltage voer 2V will not detect



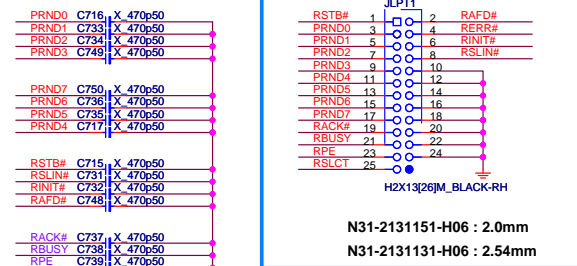
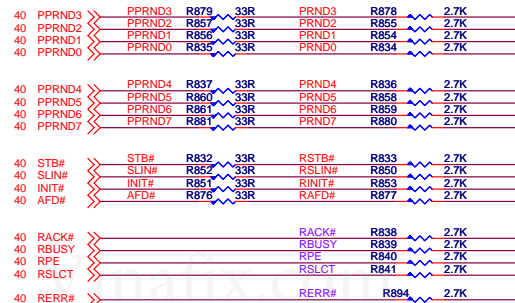
Thermal Monitor



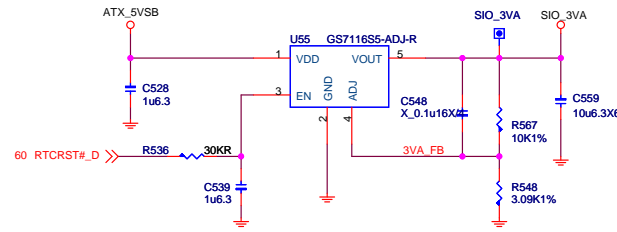
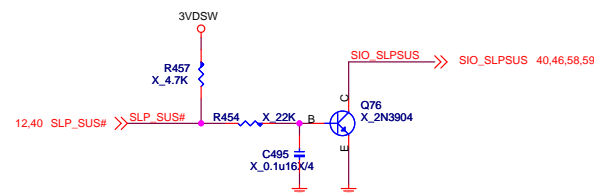
SERIAL PORT 1



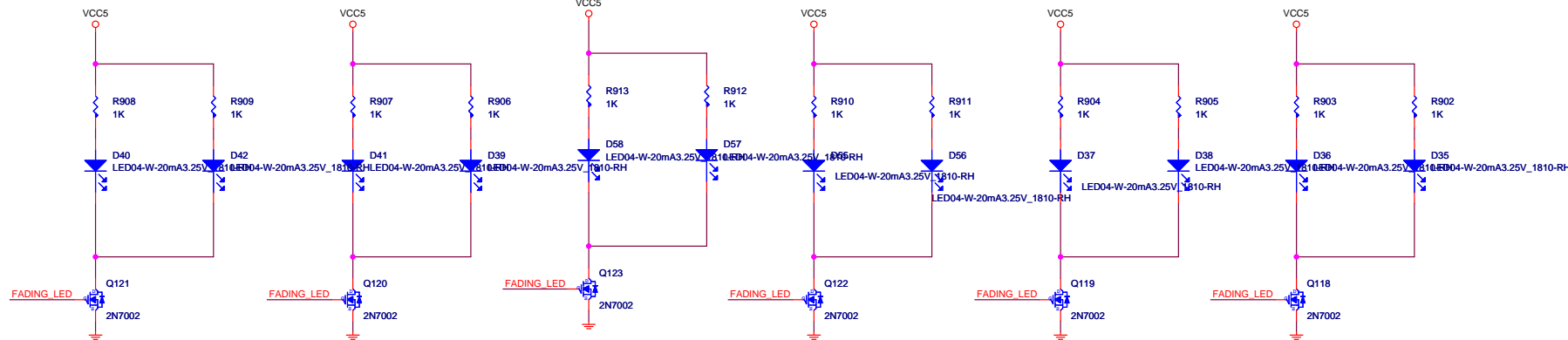
PARALLAL PORT



SLP_SUS Co-lay circuit

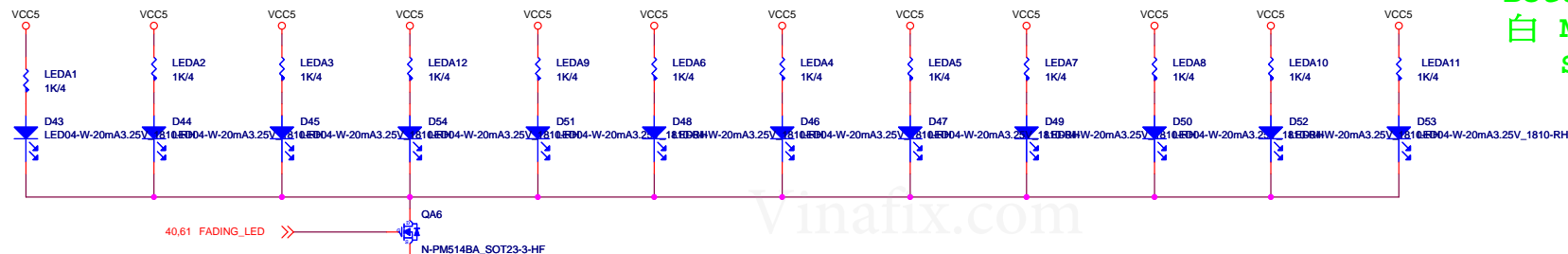


BOTTOM LED



AUDIO LED

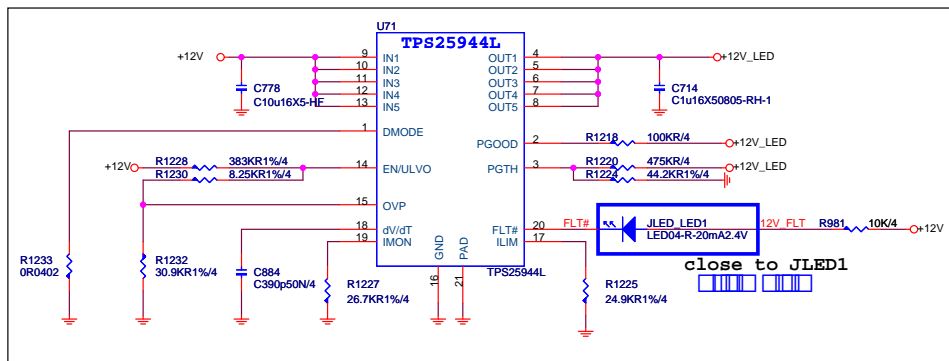
Audio moat is transparent and width 40mil



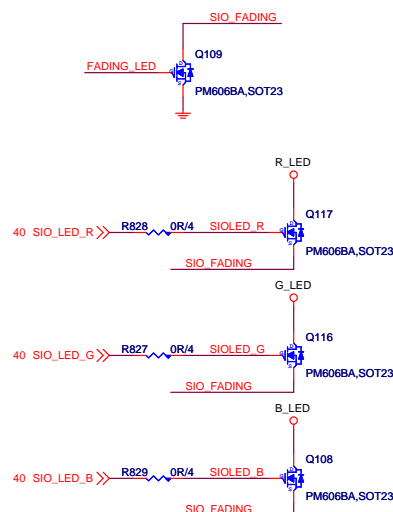
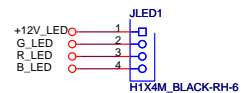
Bottom LED
白 M : D0C-040T300-H91
S : D0C-040S300-E07

LED Control by SIO

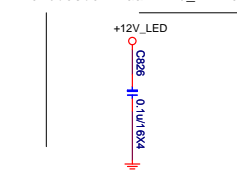
2016.07.06 Use TPS25944L



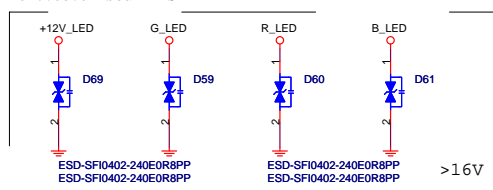
JLED1電源警告燈請擺在旁側



2016.08.02 Add +12V_LED 0.1uF



2016.08.02 stuff ESD



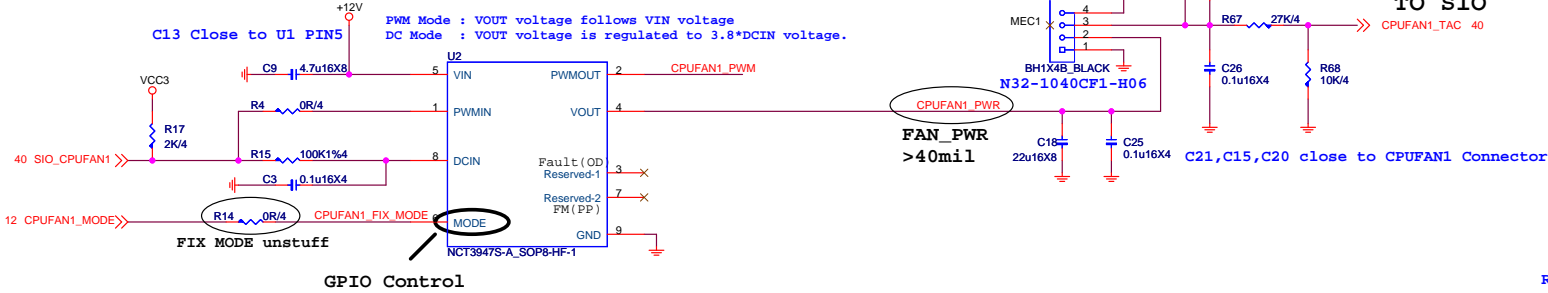
MICRO-STAR INT'L CO.,LTD

MS-7A72

| | | |
|----------------------------------|----------------------|---------|
| Size Custom | Document Description | Rev 1.0 |
| | SIO-NTC6795D-3 | |
| Date: Friday, September 23, 2016 | Sheet 42 of 66 | |

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

- 1.PWM/DC/OCF LED(現在是改成R/G/B3色LED)
- 2.GPIO可以由BIOS切換 PWM/DC MODE
- 3.OCF拉回GPIO給BIOS認
- 4.PWM OR DC FAN拉回GPIO給BIOS認
- 5.FAN轉速加快的時候由SOFTWARE 控制GPIO讓燈的變化

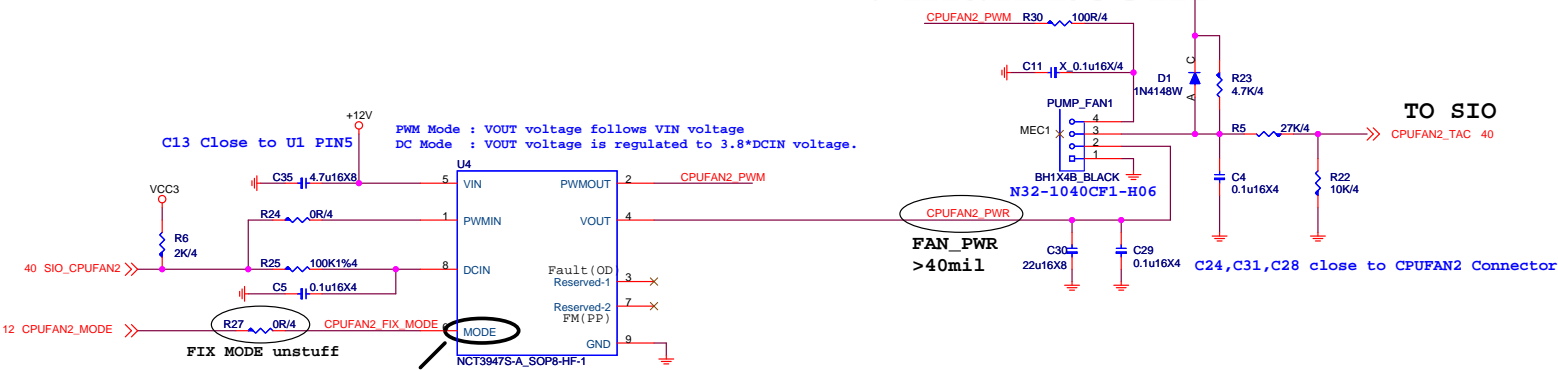


GPIO Control

| | MODE(PIN7) |
|----------|-------------------------|
| PWM MODE | HIGH |
| DC MODE | LOW |
| Default | AUTO MODE GPI(Floating) |

Internall pull up 1.65V

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



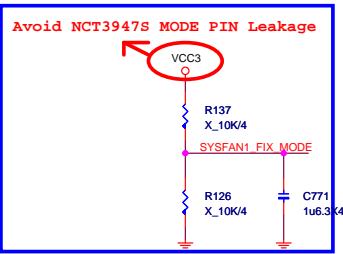
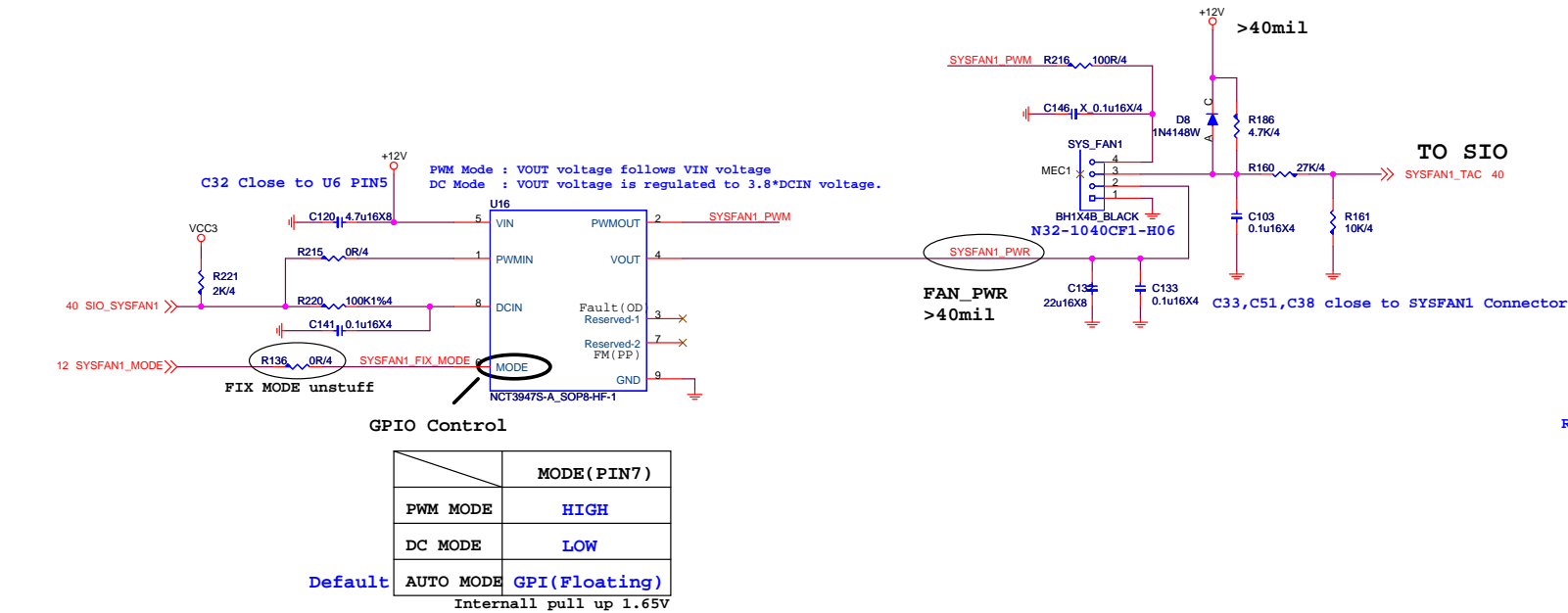
GPIO Control

| | MODE(PIN7) |
|----------|-------------------------|
| PWM MODE | HIGH |
| DC MODE | LOW |
| Default | AUTO MODE GPI(Floating) |

Internall pull up 1.65V

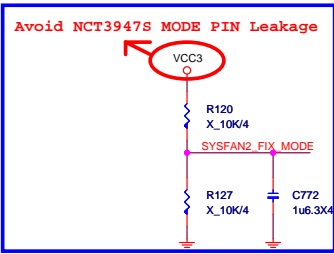
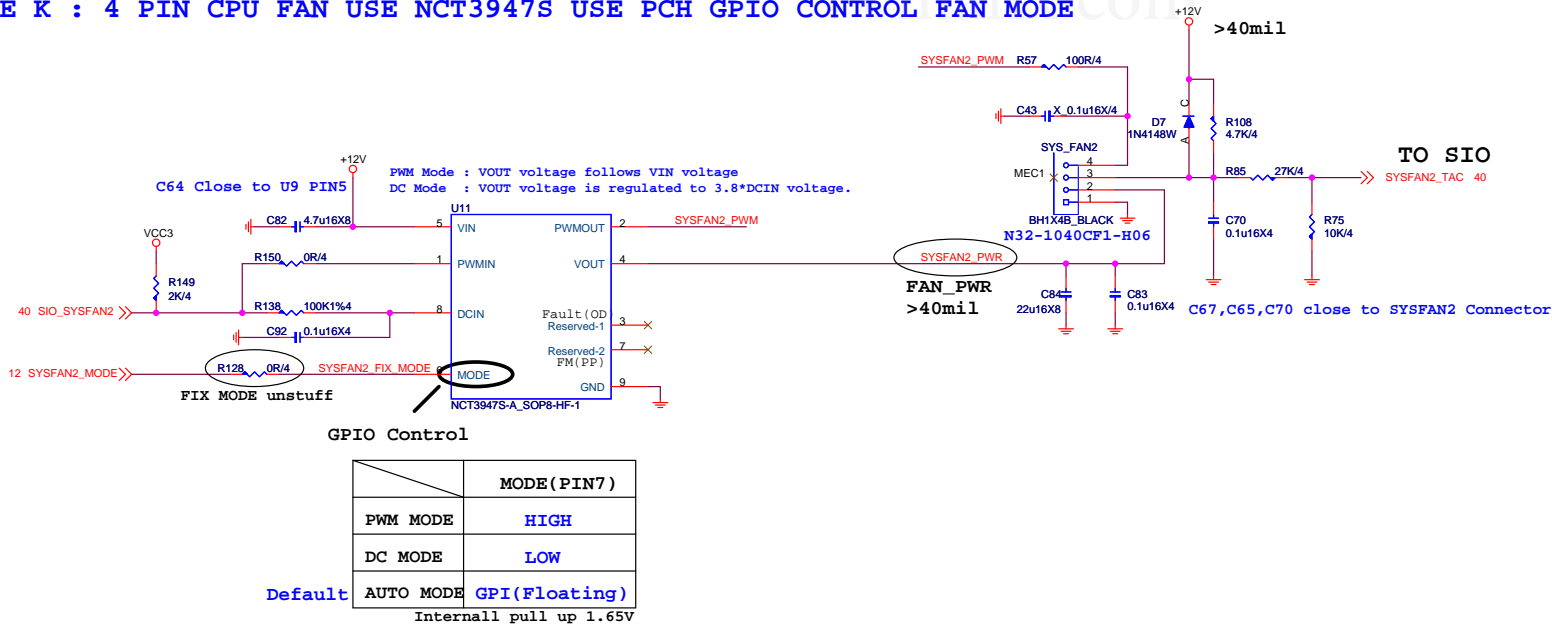
- 1.MODE : USE MODE PIN change FAN MODE(PWM or DC FAN)
- 2.FAULT : USE FAULT PIN Triger OVT/OCF Protection,LOW Atcive (Reserve NEW IC)
- 3.FM : USE FM PIN For BIOS USE to Detect PWM or DC FAN & Show information(Reserve NEW IC)

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



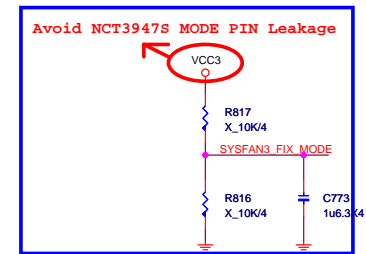
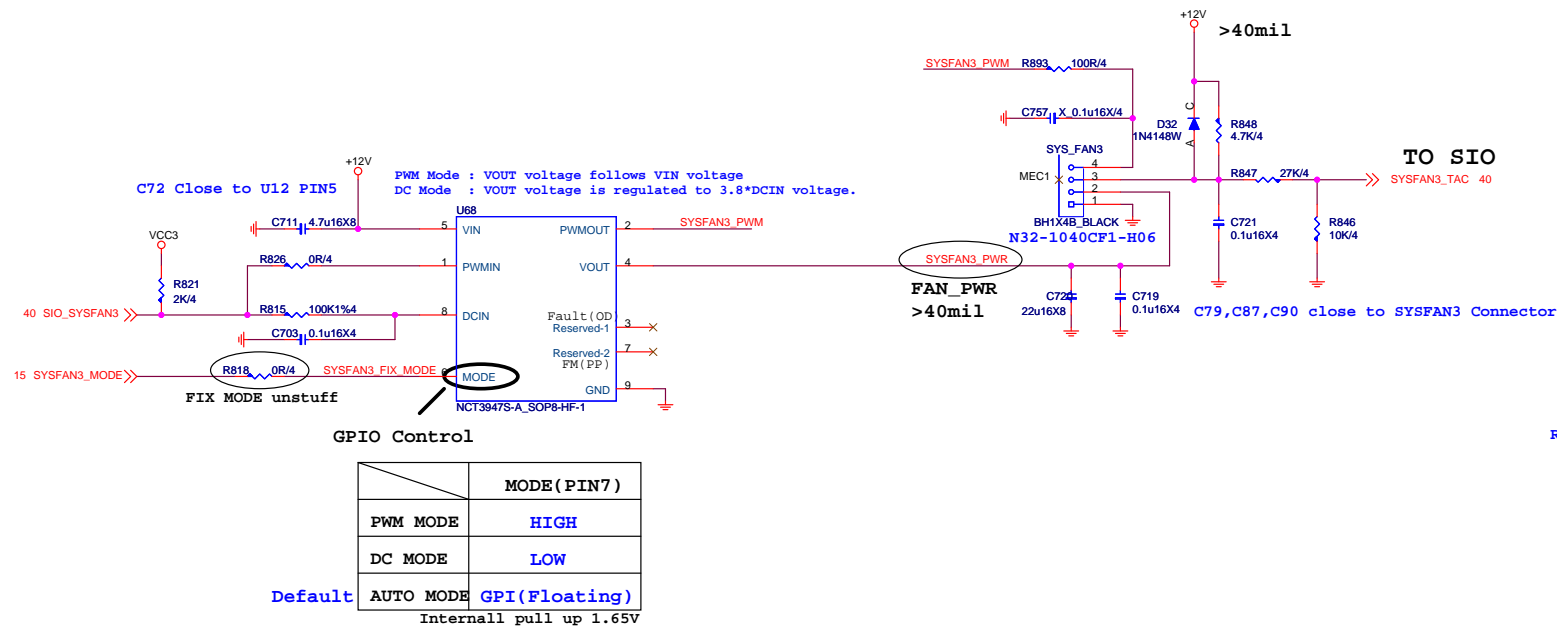
Resever For FIX DC or PWM MODE USE By PM SPEC

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



Resever For FIX DC or PWM MODE USE By PM SPEC

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

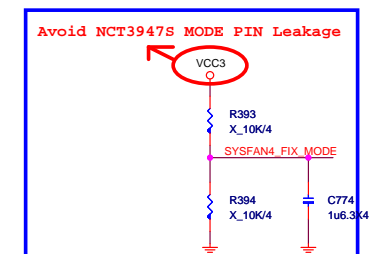
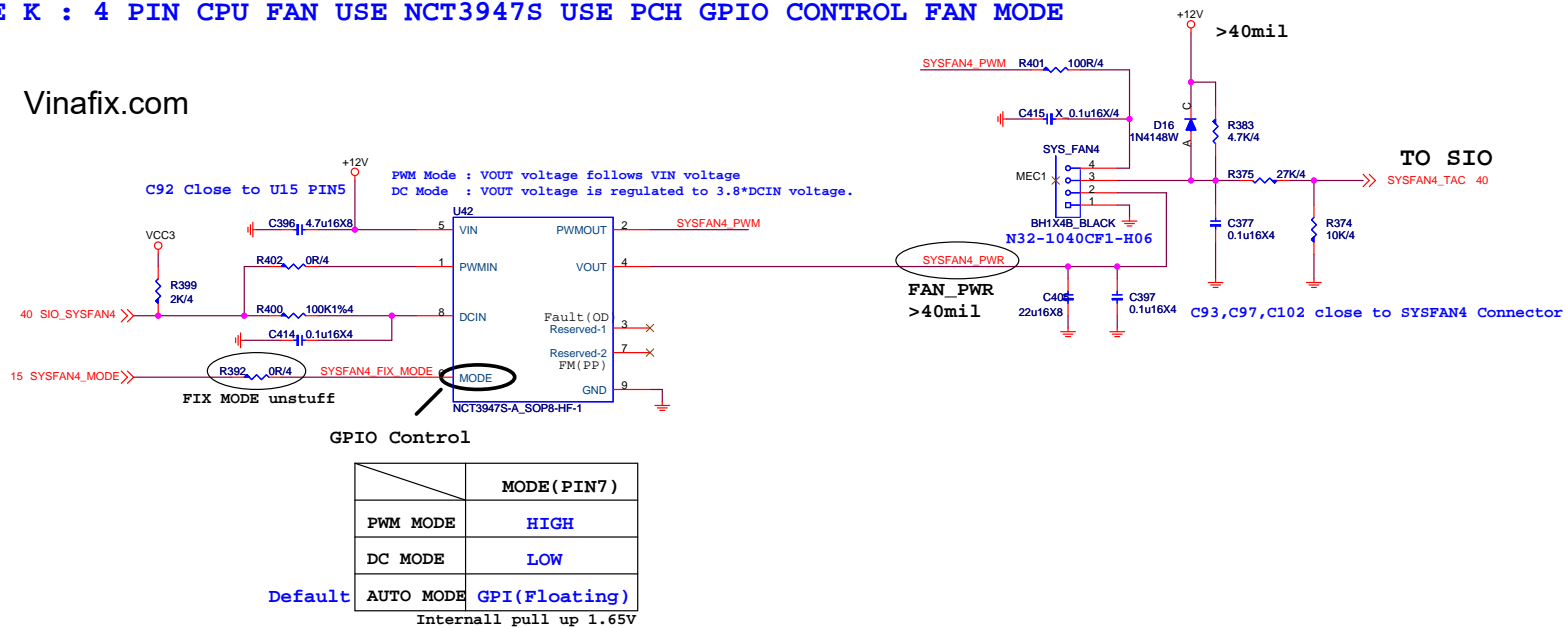


Reasever For FIX DC or PWM MODE USE By PM SPEC

Vinafix.com

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

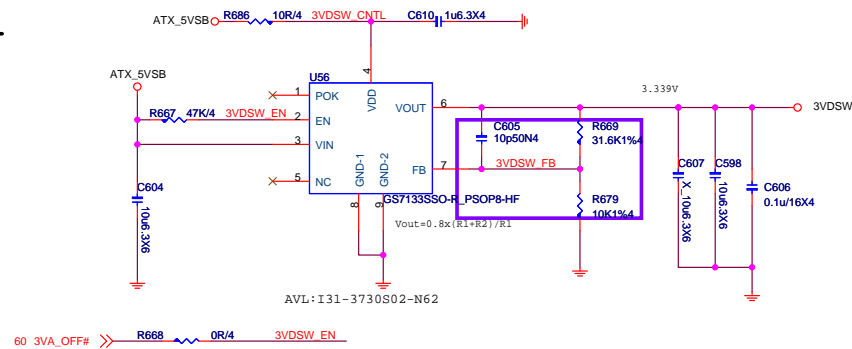
Vinafix.com



Reasever For FIX DC or PWM MODE USE By PM SPEC

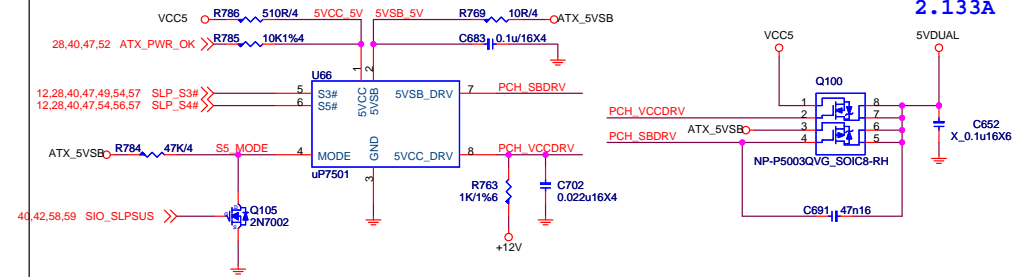
Vinafix.com

3VDSW

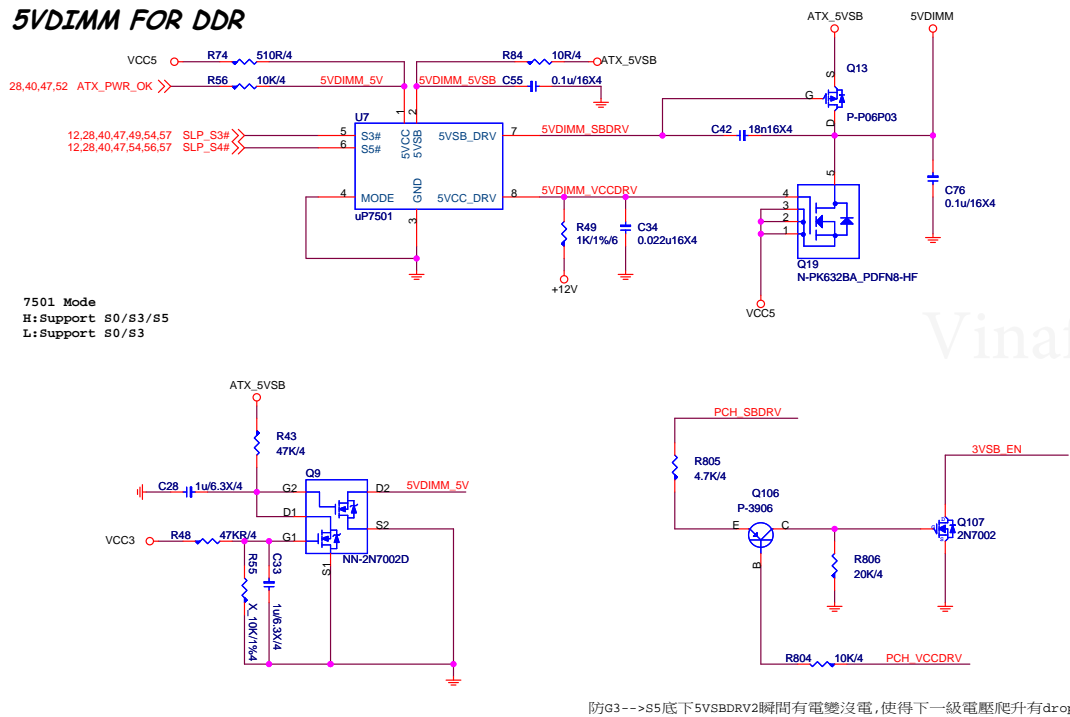


5VDUAL

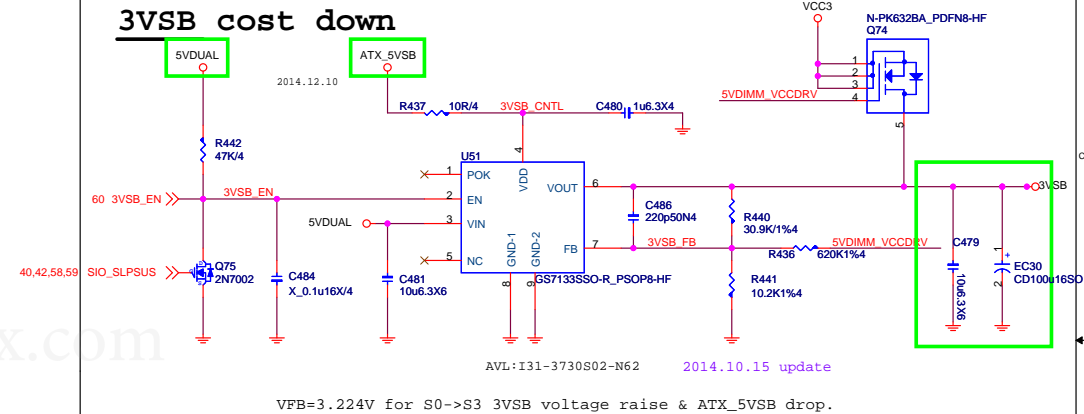
5VDUAL is power source of 1P0SB



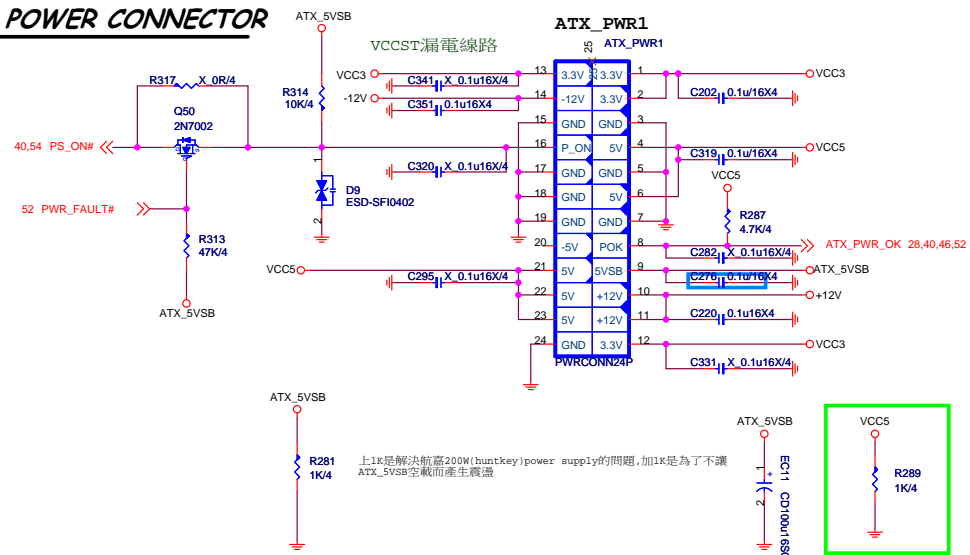
5VDIMM FOR DDR



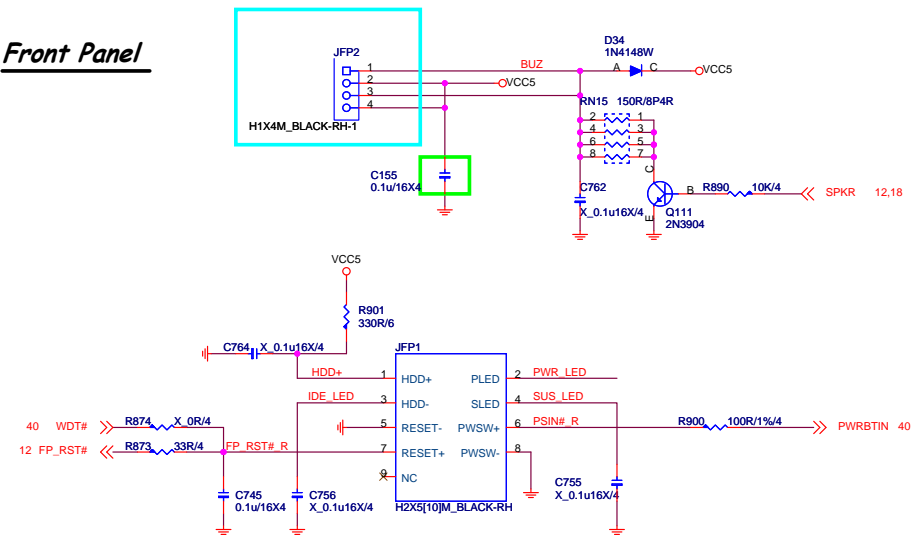
3VSB cost down



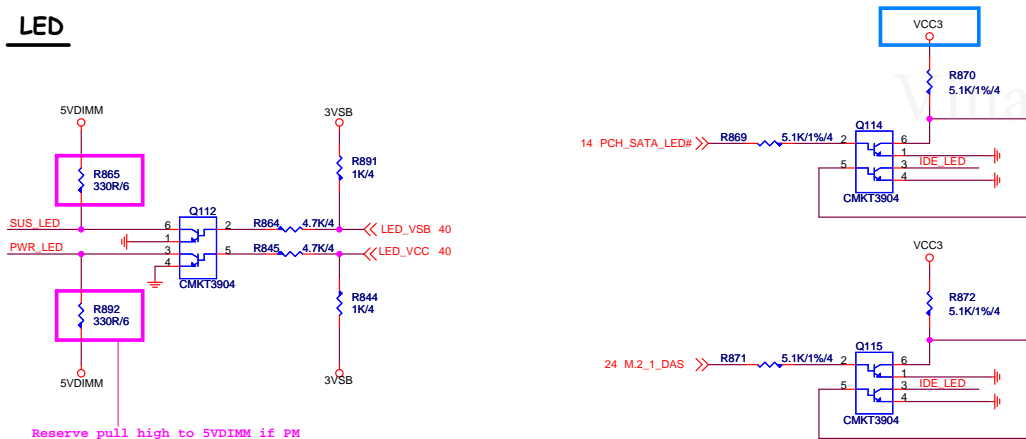
ATX POWER CONNECTOR



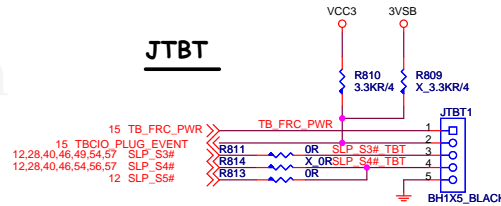
Front Panel



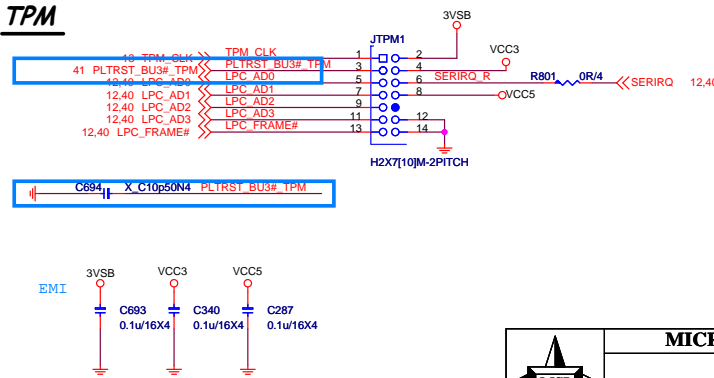
LED



JTBT



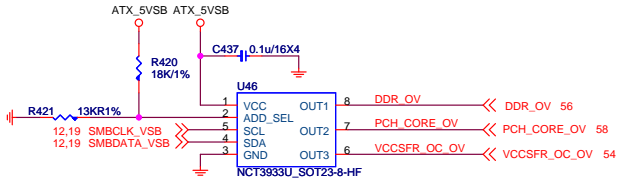
TPM



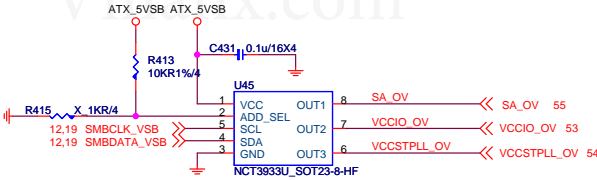
Remove Cut Power.

UPI VOLTAGE CONSOLE

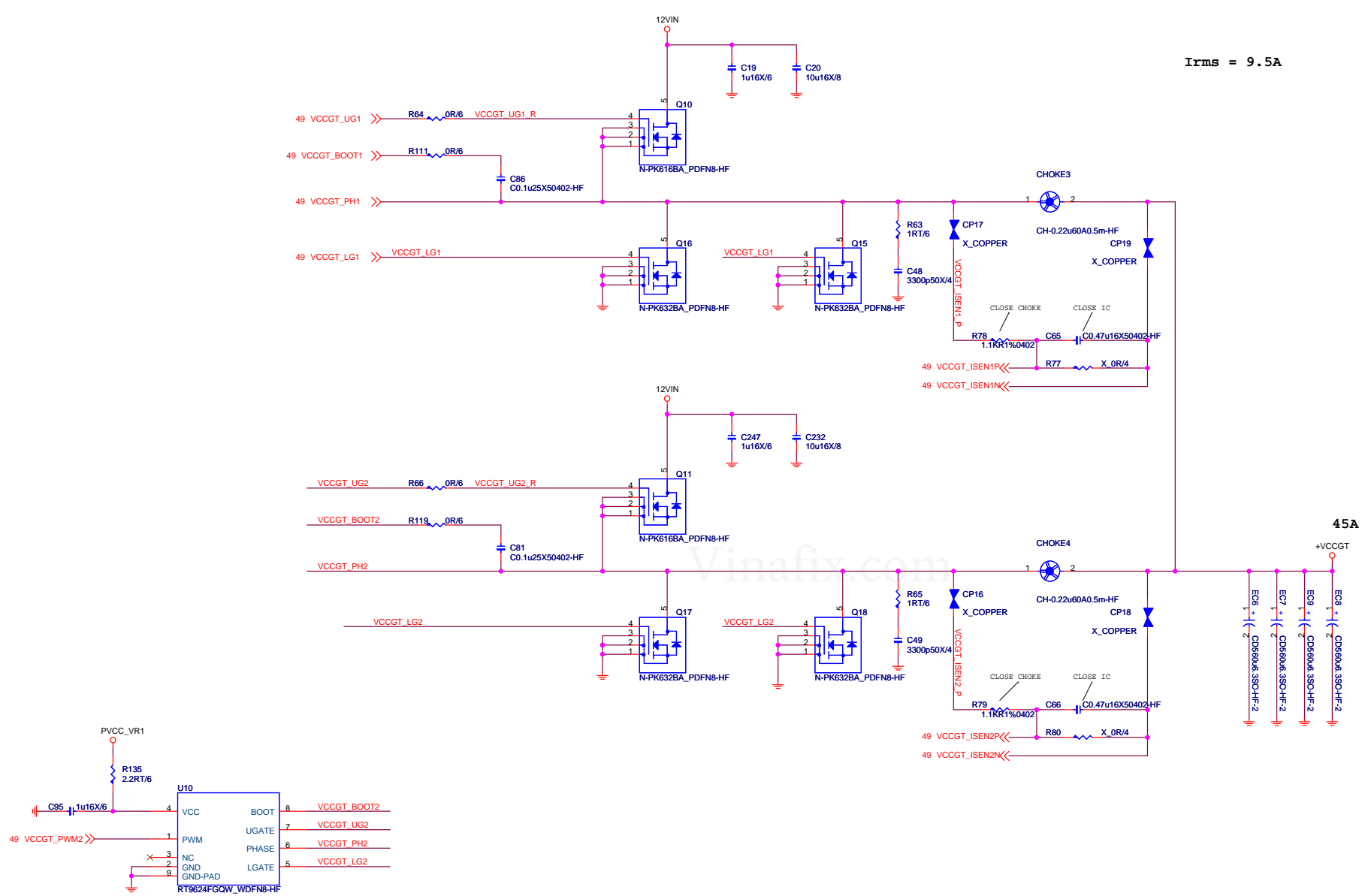
0x26:RH=18K,RL=13K



0x20:RH=10K,RL=OPEN

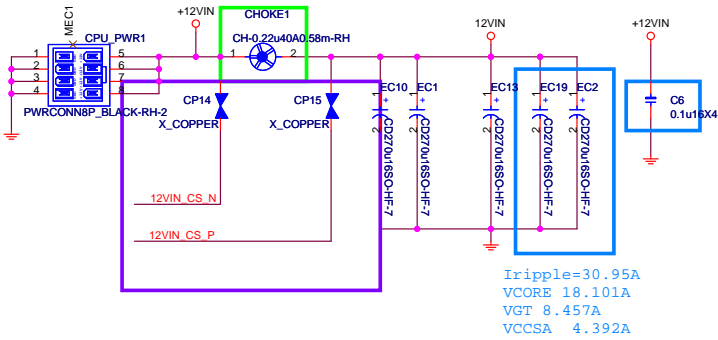


| ADDRESS | 0x2A | 0X28 | 0x26 | 0x24 | 0x22 | 0x20 |
|-----------|------|------|------|------|------|------|
| RH (KOhm) | OPEN | 3.9 | 3 | 2.2 | 1.3 | 10 |
| RL (KOhm) | 10 | 1.3 | 2.3 | 3 | 3.9 | OPEN |
| BUS_SEL | 0% | 25% | 40% | 60% | 75% | 100% |

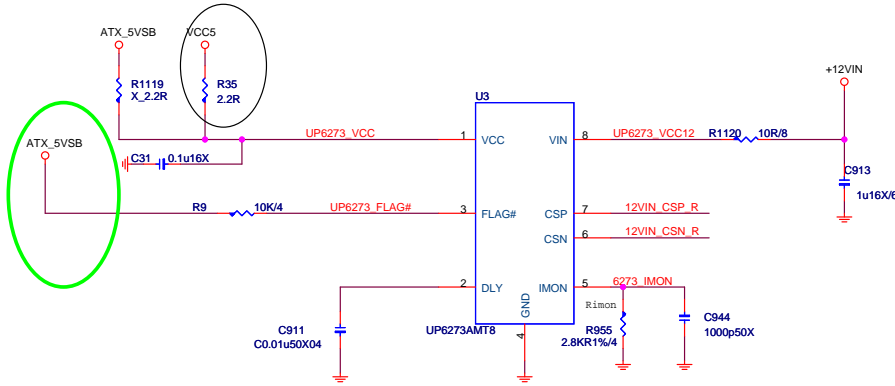


$I_{rms} = 9.5A$

45A

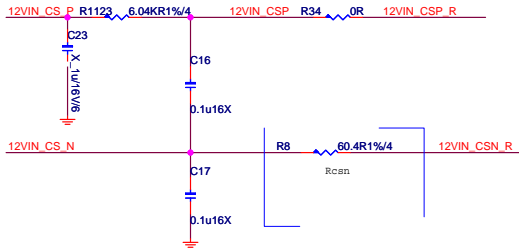
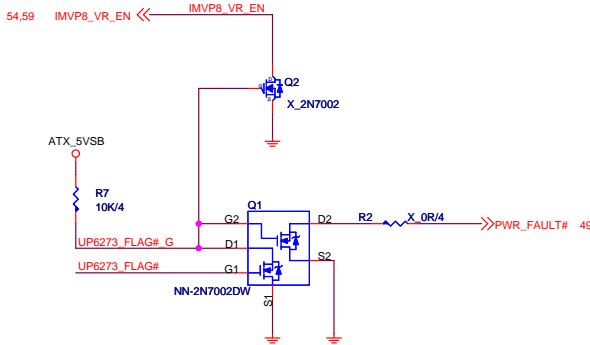


POWER METER
OCP: 120A



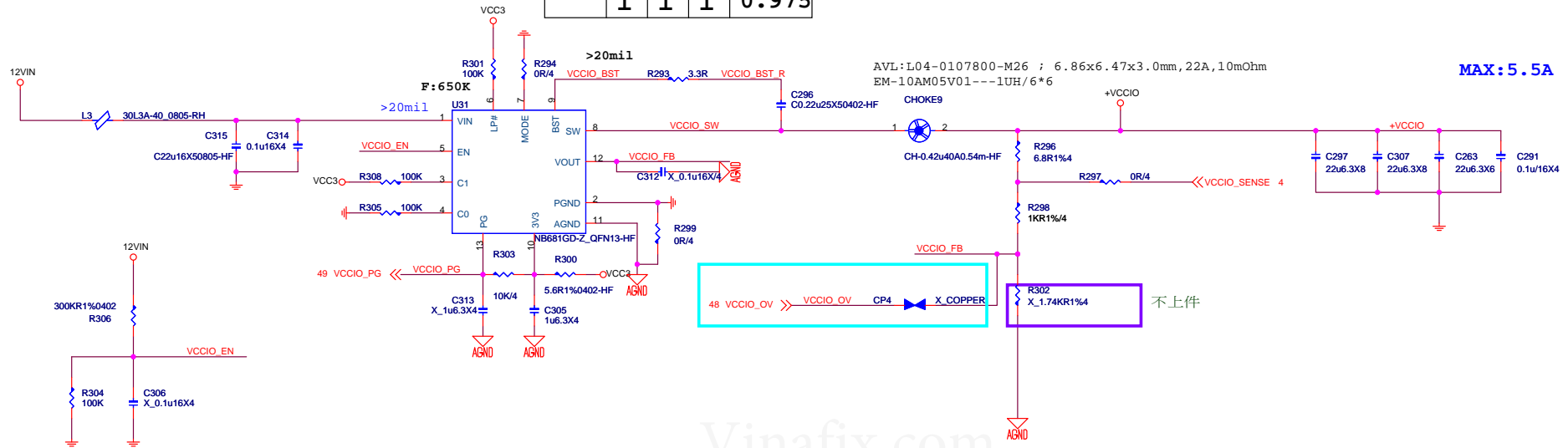
$$I_{in} = \frac{V_{mon} \cdot R_{csn}}{R_{mon} \cdot R_{dc}}$$

$V_{mon} = 1.2$
can change OCP trigger level by Rcsn and Rmon
$$(1.2 \cdot 0.2) / (10K \cdot 0.3m) = 80A$$



VCCIO
 0.95V; 5.5A
 I_{MAX} 6A
 I_{LIMIT}=8.5~9A

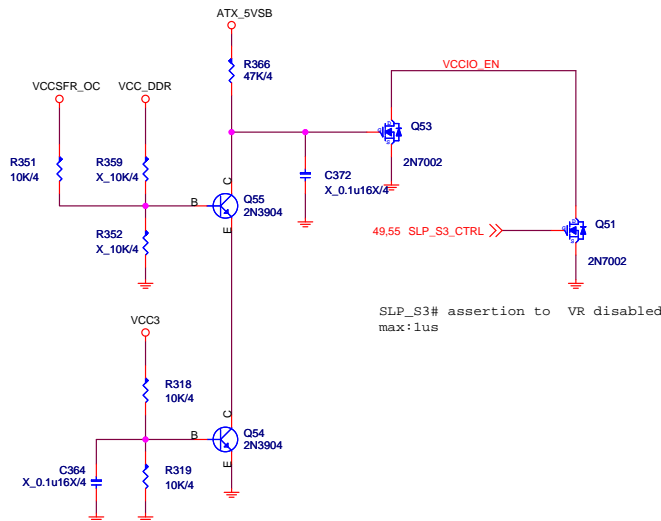
| | LP# | C1 | C0 | VOUT(V) |
|-------|-----|----|----|---------|
| VCCIO | 0 | X | X | 0 |
| | 1 | 0 | 0 | 0.85 |
| | 1 | 0 | 1 | 0.875 |
| | 1 | 1 | 0 | 0.95 |
| | 1 | 1 | 1 | 0.975 |



48 VCCIO_OV >> VCCIO_OV CP4 >> X_COPPER
 不上件

Vinafix.com

2014.12.17



SLP_S3# assertion to VR disabled
 max:1us

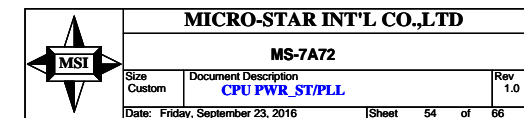
Vinafix.com

*for Gaming3/5, Classic, ECO
and H110*

For Cost down VCCST&VCCPLL merge



1.2V; 110mA



SA Power:1.05V,12.3A

Rocpset:5.6K

OCP=Rocset*Rdson(Low side)/10uA

=5.6K*3.3mohm/10uA

=18.48A

Rocs:5.76K,OCP:

D03-4C05N03-005 : 16.94A

D03-632BA0C-N03 : 17.45A

use UBIQ MOS need Check

Rdson(10V)

D03-4C05N03-005 : 3.4mohm

D03-632BA0C-N03 : 3.3mohm

D03-3056M00-U47 : 4.2mohm

up1540 LIC5/R415 no stuff

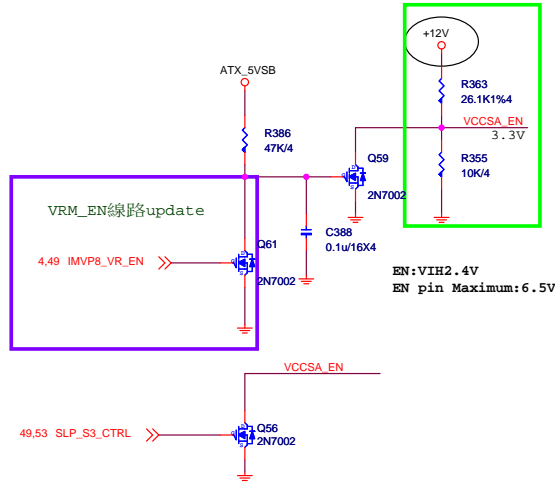
2014.12.25

for up1540:C39 is OCP set min:5K ohm
stuff 5.36K OCP SET:15.76A

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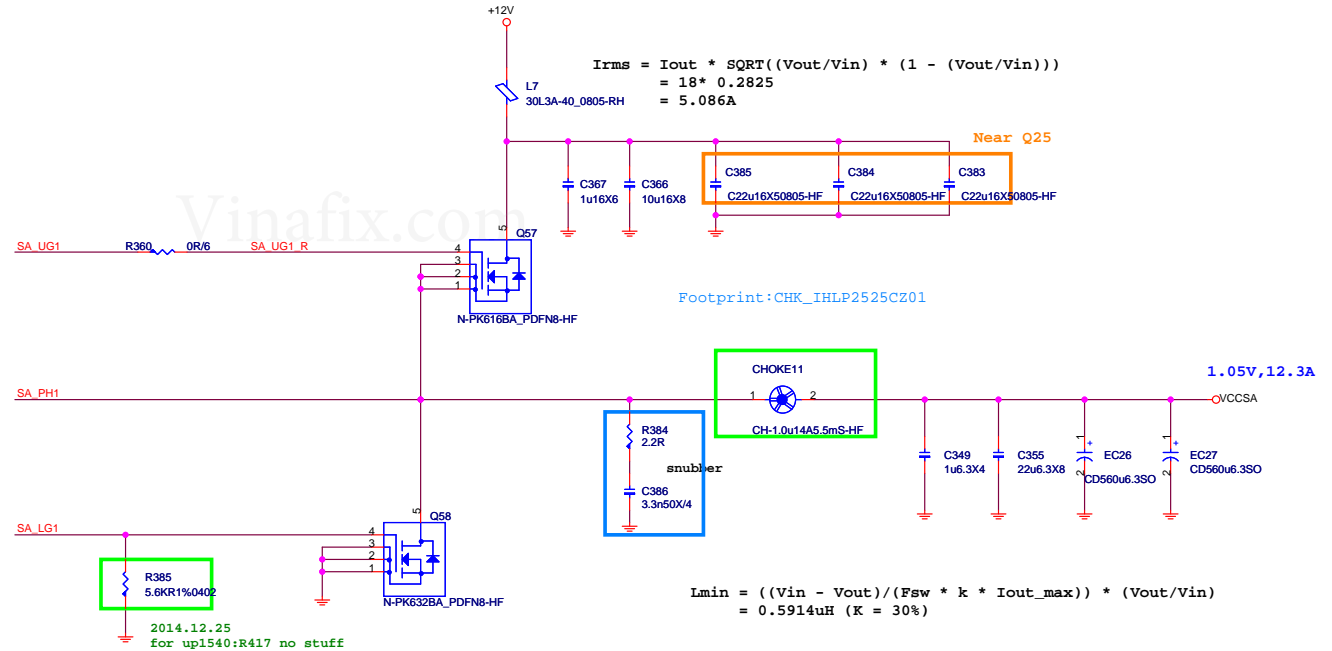
2014.08.21 update

Pull up by layout&Check level



SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.

SLP_S3# assertion to VR disabled
max:1us

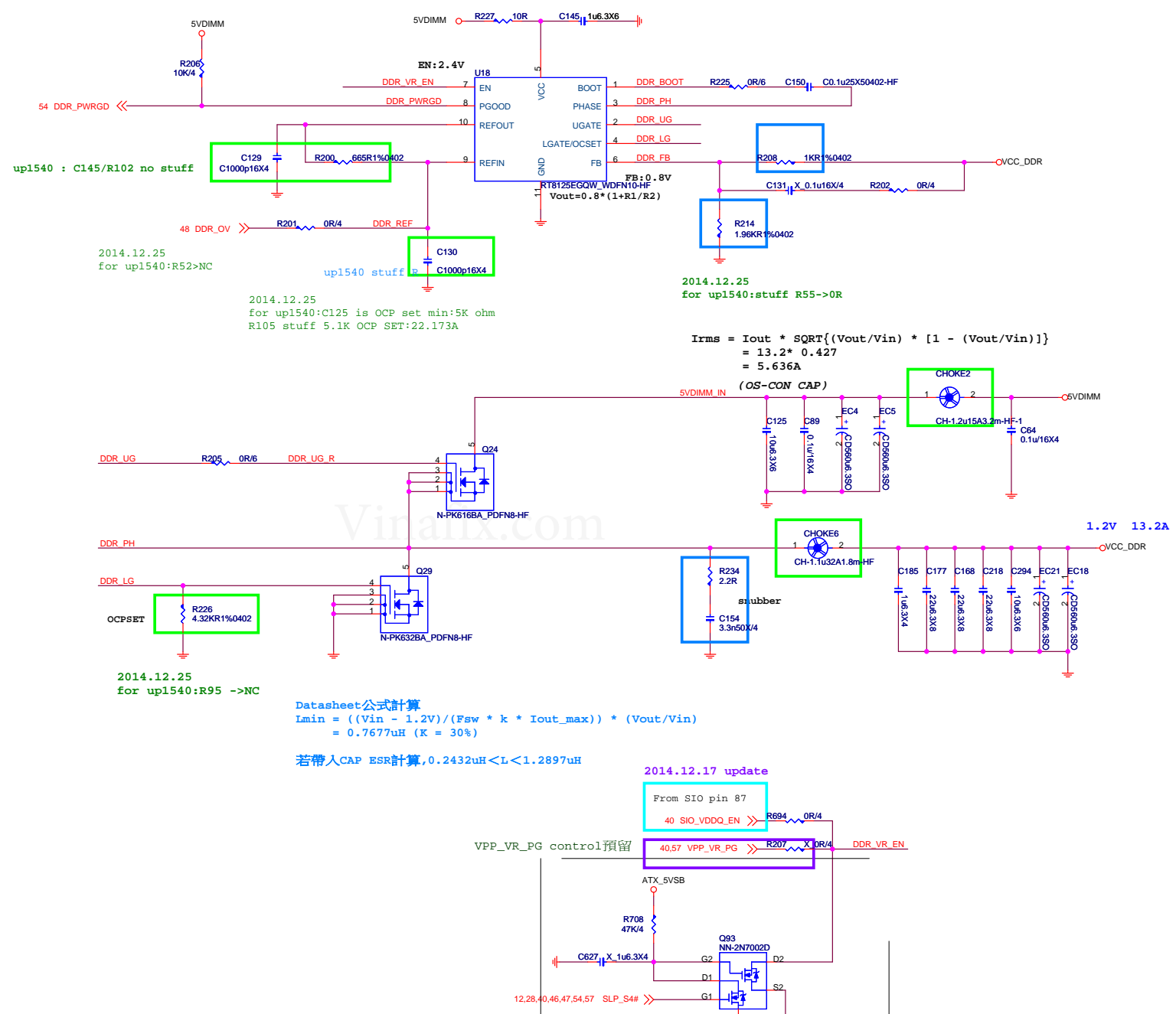


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DDR4_1.2V 2.5A+9.5A+1.2A=13.2A
 2.5A FOR CPU
 9.5A FOR 4DIMM
 1.2A FOR DDR VTT

Rocpset:4.32K
 OCP=Rocset*Rdson(Low side)/10uA
 =4.32K*4.6mohm/10uA
 =19.87A

Rdson(low)4.5V
 D03-4C05N03-O05 : 5 mohm
 D03-632BA0C-N03 : 4.6mohm
 D03-3056M00-U47 : 6.2mohm



PCH_1VSB

1.0V; 11A

Rocpset:3.48K
 OCP=Rocset*Rdson(Low side)/10uA
 =3.48K*4.6mohm/10uA
 =16A

Rocs:7.87K, OCP:
 D03-4C05N03-O05 : 15.74A
 D03-632BA0C-N03 : 17.1A
 use UBIQ MOS need Check

Rdson(Low)4.5V
 D03-3116M00-U47 : 3.6 mohm
 D03-632BA0C-N03 : 4.6mohm
 D03-3056M00-U47 : 6.2mohm

$$I_{rms} = I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))}$$

$$= 10.664 * 0.4$$

$$= 4.2656A < 5000mA$$

L04-47B7730-T15 for OC, Gaming 10, 9, 7, 5
 L04-12A7321-L65 for Gaming 3, SLI, ECO
 L04-12A7721-T15 for cost down

MAX:10.664A

$$L_{min} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out_max})) * (V_{out}/V_{in})$$

$$= 0.8335uH (K = 30\%)$$

$$V_{out} = V_{ref} * (1 + R_{821}/R_{822})$$

$$= 0.8 * (1 + 1K/3.92K)$$

$$= 0.8 * 1.2551$$

$$= 1.004V$$

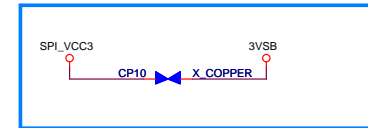
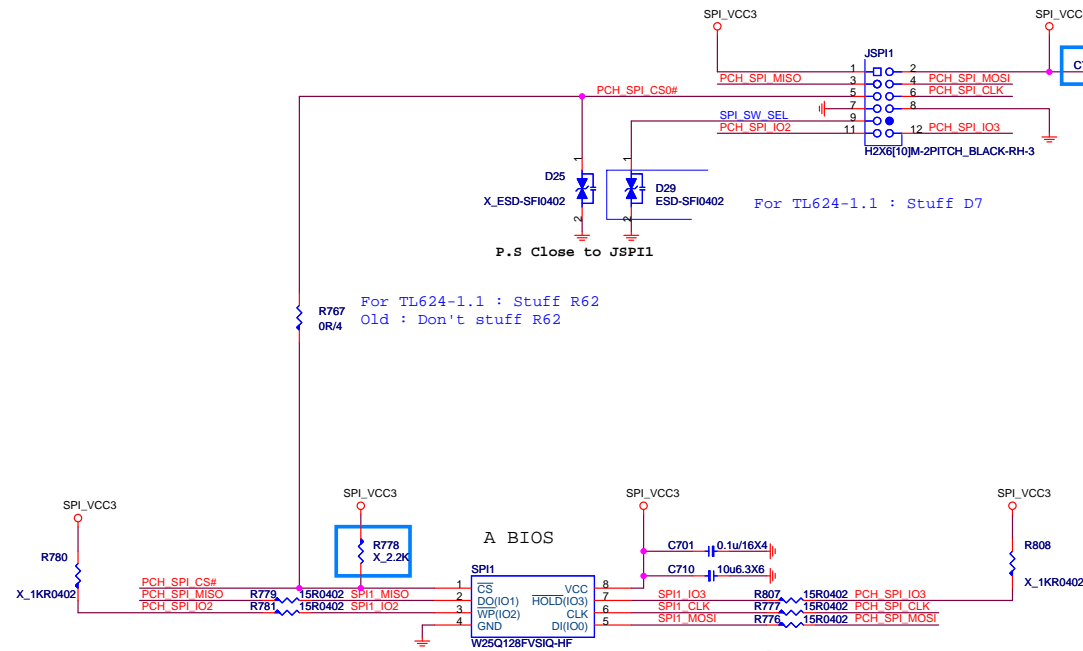
to sink/source over voltage IC.
 pin10 sink/source current capability can't over 1mA
 So max voltage can't over 1.8V.

from NCT3933

Vinafix.com

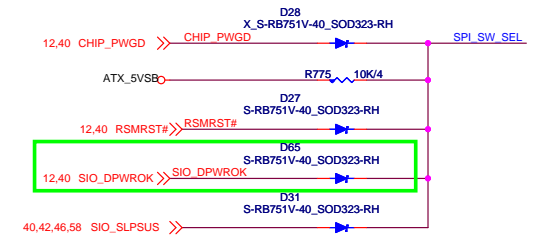
PLACE UNDER THE PCH

PCH Bottom



Module Stuff CHIP_PWGD,
But PCH_PWROK may ramp up before CHIP_PWGD.

For TL624 1.1

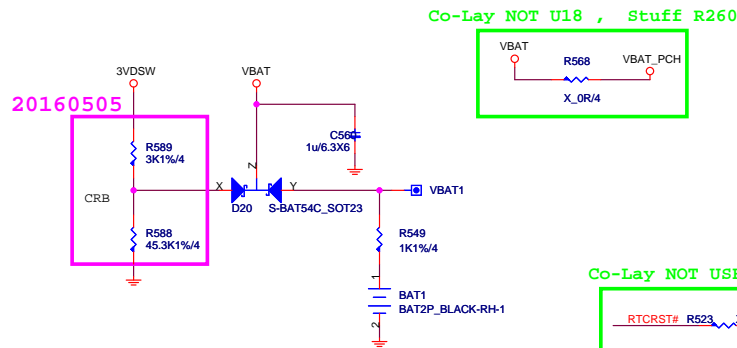


For TL624-1.1

SKYLAKE : Stuff D10/D17/R353

B85/H87 : Stuff D8/D9/R353

Others : Stuff R272



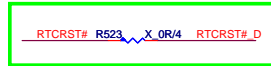
| Function 1 | | |
|------------|--------|---------|
| IN | | OUT |
| INPUT1 | INPUT2 | OUTPUT1 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |
| 0 | 0 | 0 |

Default

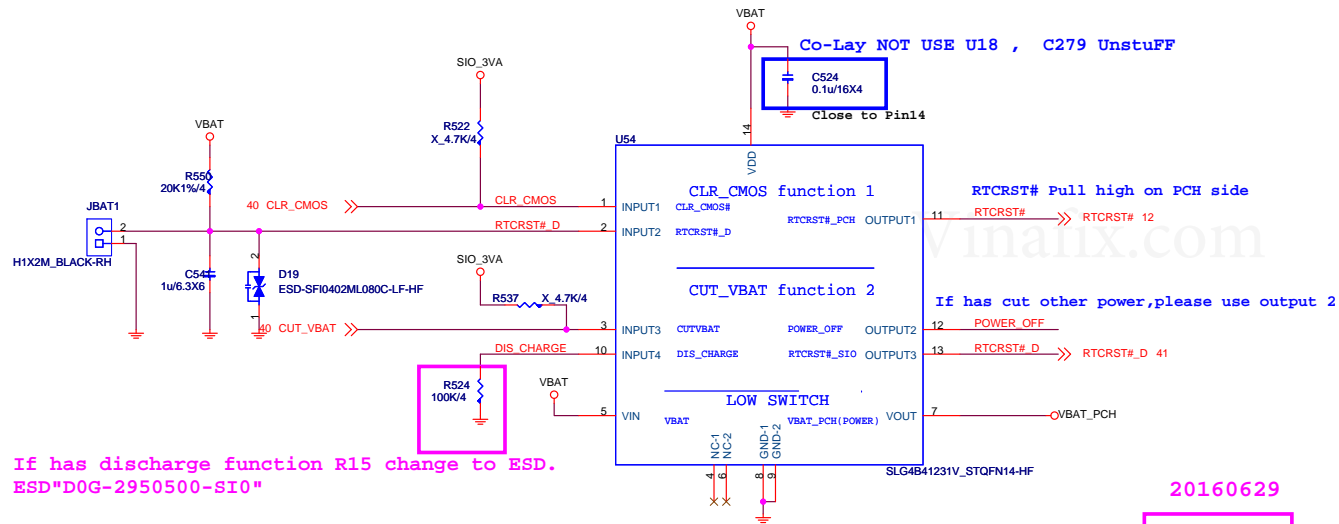
| Function 2 | | | | |
|-----------------------------|--------|---------|---------|------------------|
| IN | | OUT | | |
| INPUT3 & lowswitch EN | INPUT4 | OUTPUT2 | OUTPUT3 | VOUT |
| 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 (discharge) |
| 0 | 1 | 1 | 0 | 0 (discharge) |
| 1 | 1 | 1 | 0 | 0 (discharge) |

Default

Co-Lay NOT USE U1 , R20 STUFF

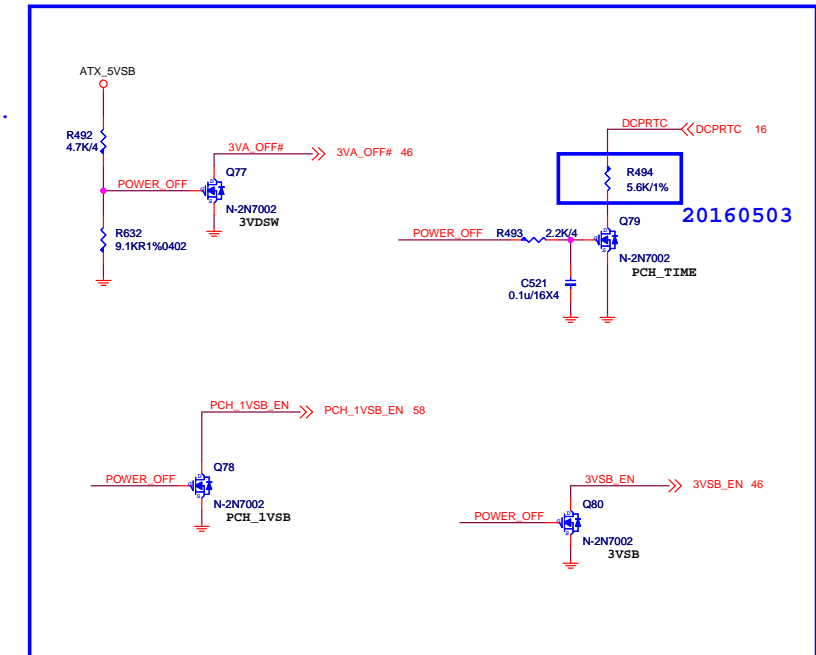


If STUFF R20 Please Check RTCRST# Double Pull High

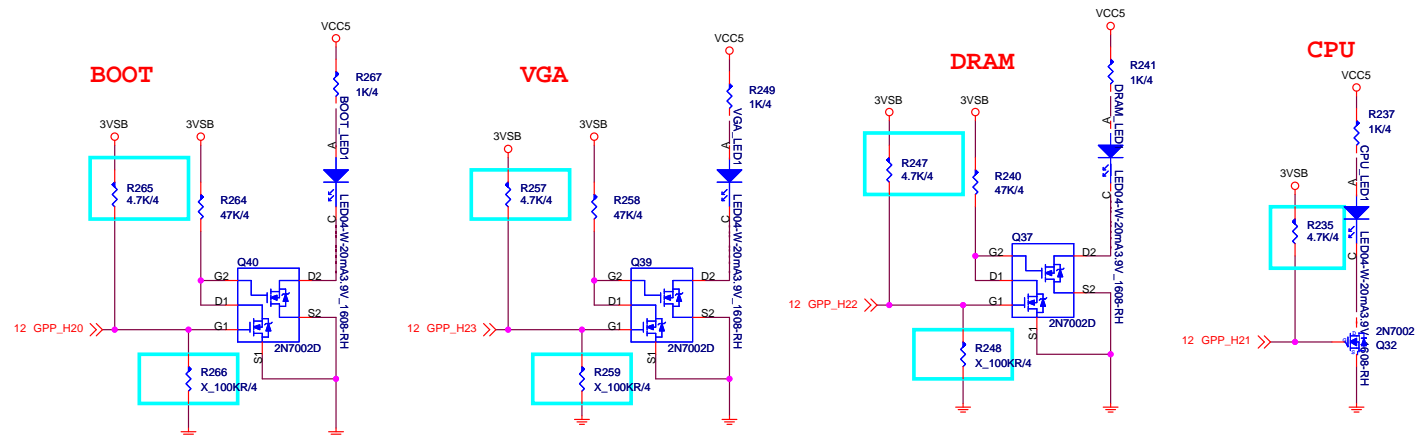


If has discharge function R15 change to ESD.
ESD"D0G-2950500-SIO"

Co-Lay NOT USE U1 , ALL UNSTUFF



EZ Debug



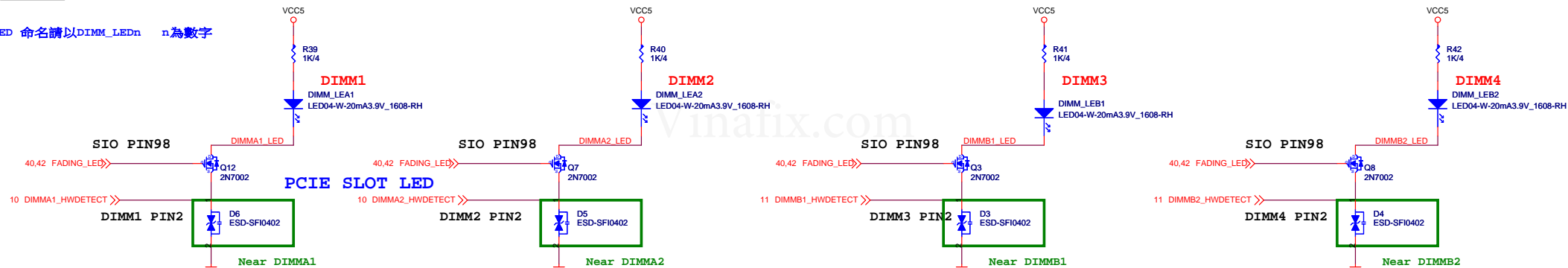
Vinafix.com

TOP LED

紅 M:DOC-040P100-H91
S:DOC-040S500-E07
白 M:DOC-040T200-H91
S:DOC-040S200-E07

DIMM

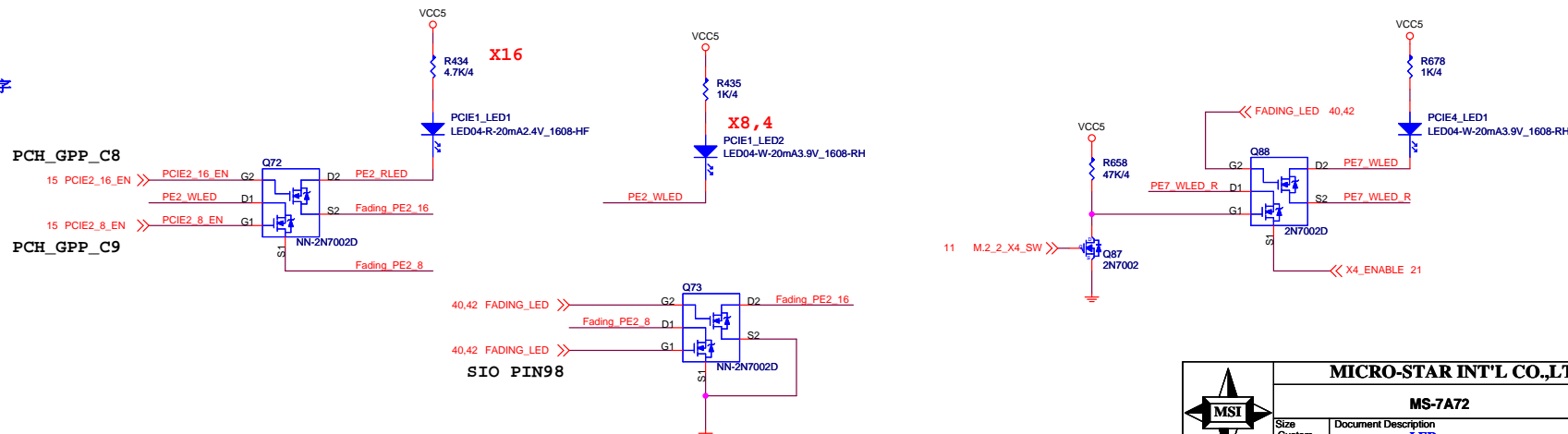
LED 命名請以DIMM_LEDn n為數字



PCIE

PCIE SLOT LED 命名請以PCIE_LEDn n為數字

| GPIO LED | GPP_C8 | GPP_C9 |
|-------------|----------------------|----------------------|
| 亮 | GPO PO HIGH | GPO PO HIGH |
| 滅 | GPI (default LOW) | GPI (default LOW) |



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PCB



PD0-07A7210-G37, 精成-深圳, 23, 寶安恩斯邁廠 (MSIS)
PD0-07A7210-G37, 精成-深圳, 77, 寶安恩斯邁廠 (MSIS)
PD0-07A7210-E48, 競華, 23, 寶安恩斯邁廠 (MSIS)
PD0-07A7210-E48, 競華, 77, 寶安恩斯邁廠 (MSIS)

CPU Socket

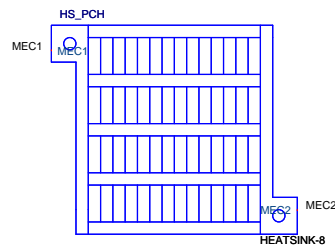


HDMI Virtual Part Number

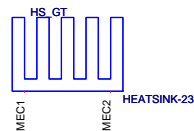
Battery



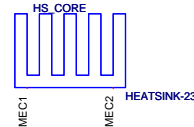
BIOS Label



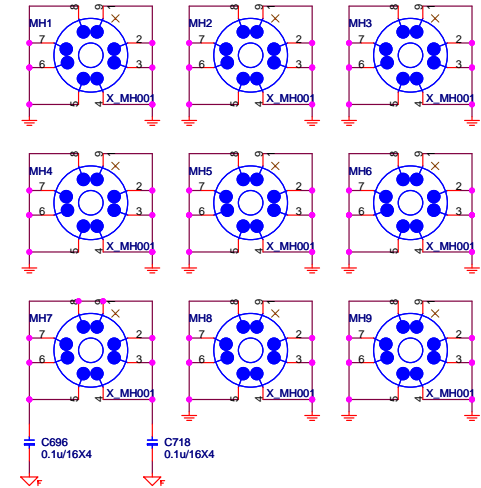
MOS1 Heatsink



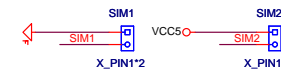
MOS2 Heatsink



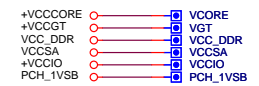
Mounting Holes



Simulation



Test point



Optical Fiducial Marks-120

